CMX90A004 2W 860 – 960MHz Power Amplifier

Description

The CMX90A004 is a two-stage, fully matched MMIC PA delivering +32.5 dBm of saturated power for use in the 860 – 960 MHz frequency range, applicable to license-free bands.

The device is optimised for maximum efficiency at collector voltages of 2.7 – 4.5 V, making it suitable for systems operating from a single-cell Li-Ion battery.

CMX90A004 is highly integrated for ease of use, minimising external component count and reducing board area. RF input and output matching is incorporated on-chip, as well as active bias circuitry and an input DC-blocking capacitor.

Using advanced GaAs HBT technology to provide a combination of high efficiency and gain, the CMX90A004 is intended as a high-power final stage ISM band PA in wireless applications.

4x4mm VQFN-16 Package

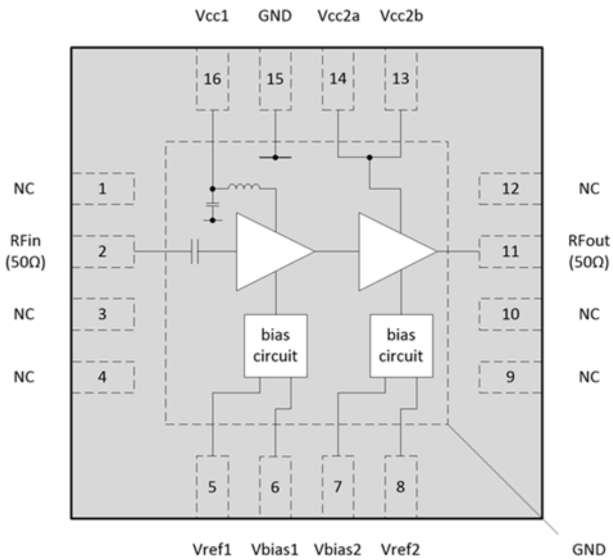
Product Features

- Frequency range 860 – 960 MHz
- Supply voltage – 2.7 – 4.5 V
- Output power 32.5 dBm @ 3.6 V
- Input and output matched to 50 Ω
- Small signal gain 30 dB
- High PAE of 49%
- Shut-down and output power control

Applications

- Automatic meter readers (AMR)
- Smart meters
- Wireless modules
- UHF RFID readers
- Final stage PA
- Internet of Things (IoT)
- 868 / 915 MHz ISM
- Li-Ion battery powered systems

Block Diagram



Ordering Information

Part Number	Description
CMX90A004Q7-R710	7” Reel with 1,000 pieces
CMX90A004Q7-R350	13” Reel with 5,000 pieces
EV90A004	Evaluation board

Absolute Maximum Ratings

Parameter	Rating
RF Input Power	+13 dBm
Device Voltage (Vcc1, Vcc2)	+5 V
Pdiss	2.68 W @Tc = +85 °C
Case Temperature (Tc)	-40 to +85 °C
Junction Temperature (Tjmax)	160 °C (MTTF = 10^6 hours)
Storage Temperature	-40 to +125 °C
ESD Sensitivity	HBM 250 V (Class 1A); CDM 250 V (Class C1)
MSL Level	Level 3

Exceeding the maximum ratings may result in damage or reduced device reliability.

Thermal Characteristics

Parameter	Rating
Thermal Resistance (Rjc)	28 °C/W

Thermal resistance is junction-to-case, where case refers to the exposed die pad on the backside which is in contact with the board.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Operating Frequency Range	860		960	MHz
Quiescent Current (Icq)		78		mA
Case Temperature (Tc)	-40		+85	°C
Device Voltage (Vcc1, Vcc2)	2.7	3.6	4.5	V
Bias Voltage (Vbias1, Vbias2)	2.7	3.3	4.5	V
Current into Vref1		2.78	5	mA
Current into Vref2		2.88	5	mA

The device will be tested under certain conditions, but performance is not guaranteed over the full range of recommended operating conditions.

ESD Caution

CMX90A004 incorporates ESD protection circuitry. However, ESD precautions are strongly recommended for handling and assembly. Ensure that devices are protected from ESD in antistatic bags or carriers when being transported. Personal grounding is to be worn at all times when handling these devices.

RoHS Compliance

All devices supplied by CML Microcircuits are compliant with RoHS directive (2011/65/EU), containing less than the permitted levels of hazardous substances.

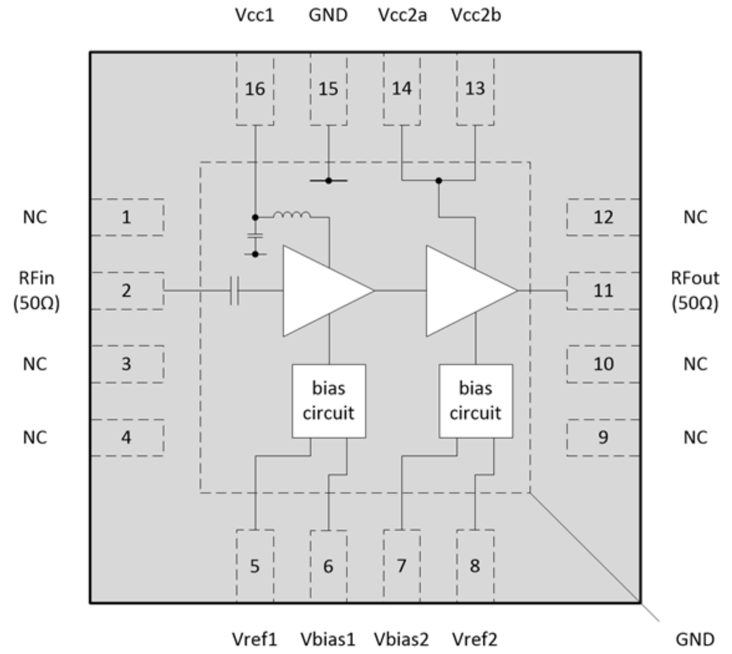
Electrical Specification

Measured result on the EV90A004 EVB will include losses in the PCB tracking and DC blocking capacitor (typically 0.2 dB output loss from device to output connector).

Zo = 50 Ω, Vcc = +3.6 V, Vbias = +3.3 V, Vref = +3.3 V, Pin = +5 dBm, Ta = +25 °C (unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Units
Frequency		860		960	MHz
Psat			32.5		dBm
Small Signal Gain	Pin = -20 dBm		30		dB
PAE	915MHz		49		%
Current Consumption (Icc)	915MHz		1.0		A
Input Return Loss	Pin = -20dBm		-10		dB
Output Return Loss	Pin = -20dBm		-7		dB
2Fo			-27		dBc
3Fo			-43		dBc
Ruggedness	Output VSWR = 5:1, all phase angles up to 4 V Output VSWR = 3:1, all phase angles at 4.5 V		No device damage or permanent performance degradation		
Stability	Output VSWR = 5:1, all phase angles at 4 V		No spurious emissions observed		
Quiescent Current (Icq)	RF off		78		mA
Standby Current	Vcc current in standby mode, RF off		5		uA
Vbias1, 2	Supply voltage for active bias circuitry		3.3		V
Vbias Current	Vbias 1 & 2 total current. RFin = +5 dBm		12		mA
Vctrl1, 2	Vref pins require external 270R series resistors		3.3		V
Vctrl1, 2 (Standby)	PA placed into standby mode	0		1.5	V
Vctrl Current	Vctrl 1 & 2 total current. RFin = +5 dBm		5.66		mA
Output Power Control	Vref can be used to ramp between min and max output power.		70		dB
Turn-On Time	Vref = 0 V to 3.3 V		600		ns
Turn-Off Time	Vref = 3.3 V to 0 V		60		ns

Pin Assignments



Top View

Pin	Name	Description
1	NC	Connect to GND
2	RFin	RF input. Internally matched to 50 Ω with integrated DC-blocking capacitor.
3	NC	Connect to GND
4	NC	Connect to GND
5	Vref1	Sets bias current to driver stage. Regulated voltage and external series resistor required. Also used for on/off and power control.
6	Vbias1	Supplies base current to driver stage
7	Vbias2	Supplies base current to final stage
8	Vref2	Sets bias current to final stage. Regulated voltage and external series resistor required. Also used for on/off and power control.
9	NC	Connect to GND
10	NC	Connect to GND
11	RFout	RF output. Internally matched to 50 Ω. External DC-blocking capacitor required.
12	NC	Connect to GND
13	Vcc2b	Collector supply to final stage
14	Vcc2a	Collector supply to final stage
15	GND	Connect to GND
16	Vcc1	Collector supply to driver stage with integrated RF choke
Die pad	GND	DC and RF ground. Exposed die pad must be connected to GND.

Notes
CML recommends that all no connect (NC) pins are connected to ground.
The bottom exposed die pad must be connected to the ground plane on the board, note guidance given in the application information section.

Typical Performance

The following plots show typical performance characteristics of CMX90A004 measured on the evaluation board (Part Number EV90A004). The measurements include input and output circuit losses associated with the evaluation board.

Test conditions unless otherwise noted:-

Vcc = +3.6 V, Vbias = Vctrl = +3.3 V, Ta = +25 °C, Zo = 50 Ω

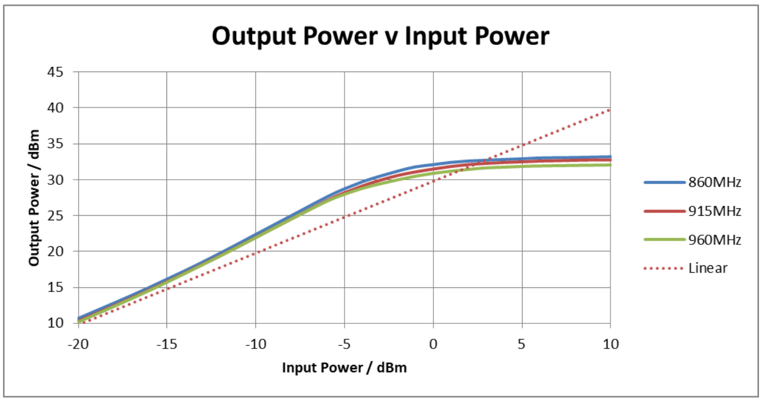


Figure 1: Output Power v Input Power

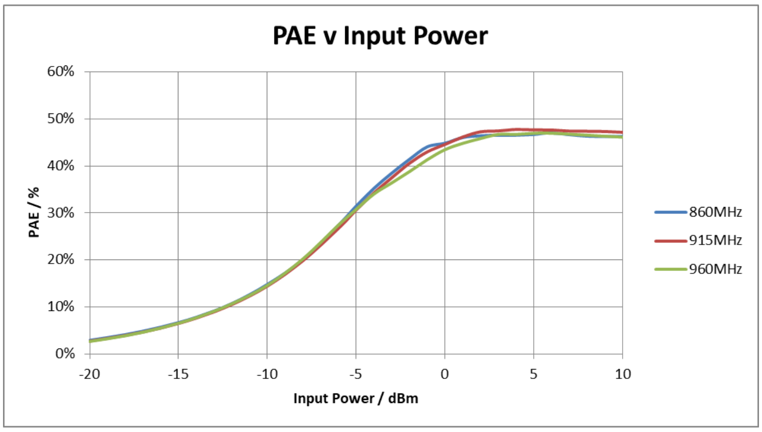


Figure 2: PAE v Input Power

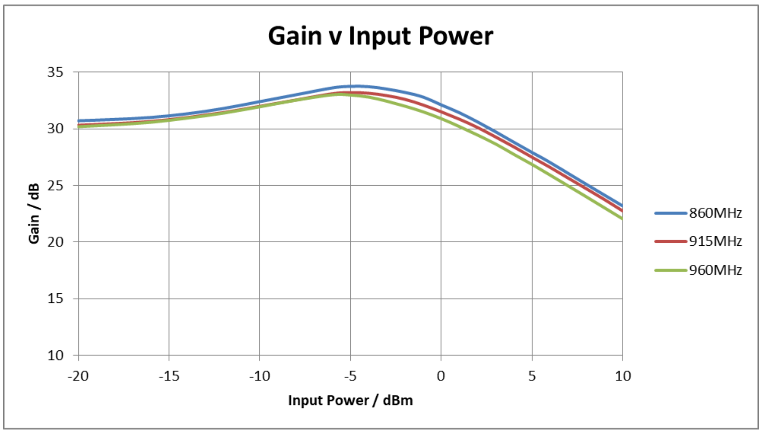


Figure 3: Gain v Input Power

Test conditions unless otherwise noted:-

Vcc = 3.6 V, Vbias = 3.3 V, Vctrl = 3.3 V, Zo = 50 Ω

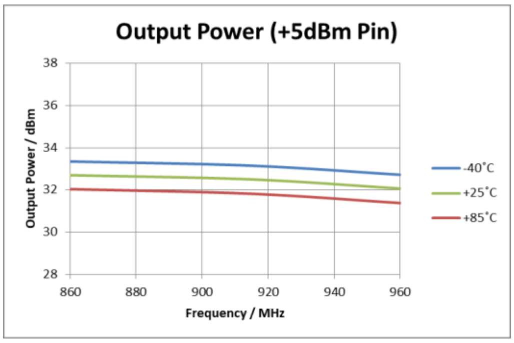


Figure 4: Output Power (+5 dBm Pin)

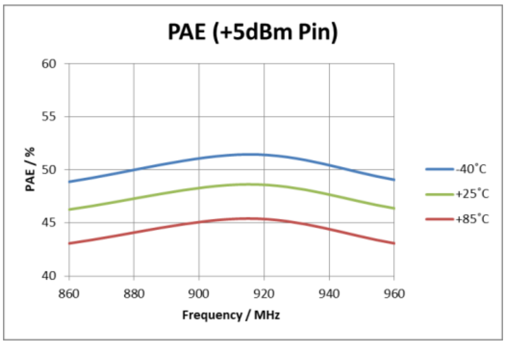


Figure 6: PAE (+5 dBm Pin)

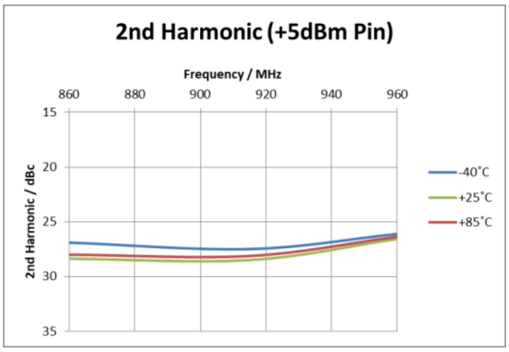


Figure 8: 2nd Harmonic (+5 dBm Pin)

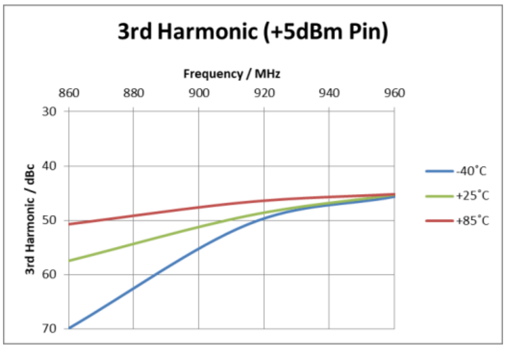


Figure 10: 3rd Harmonic (+5 dBm Pin)

Ta = 25˚C, Vbias = 3.3 V, Vctrl = 3.3 V, Zo = 50 Ω

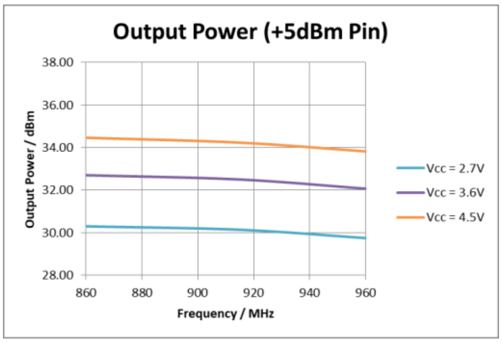


Figure 5: Output Power (+5 dBm Pin)

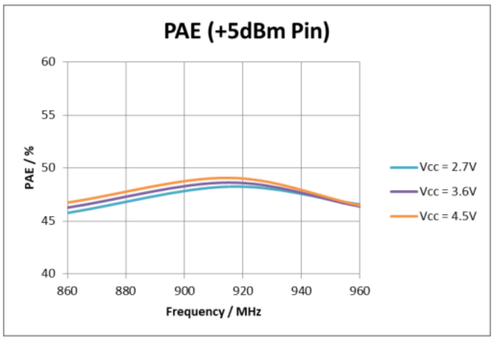


Figure 7: PAE (+5 dBm Pin)

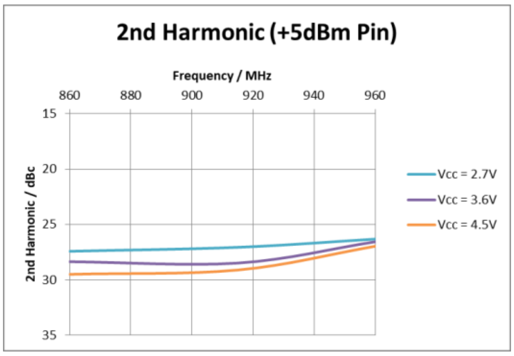


Figure 9: 2nd Harmonic (+5 dBm Pin)

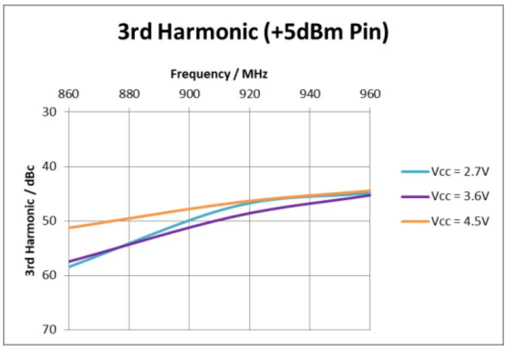


Figure 11: 3rd Harmonic (+5 dBm Pin)

Test conditions unless otherwise noted:-

Vcc = 3.6 V, Vbias = 3.3 V, Vctrl = 3.3 V, Zo = 50 Ω

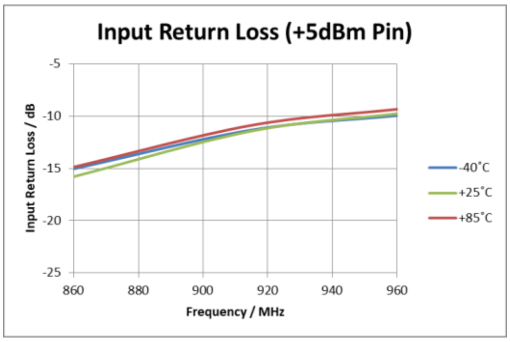


Figure 12: Input Return Loss (+5 dBm Pin)

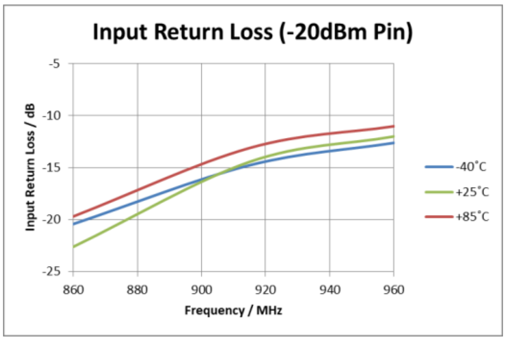


Figure 14: Input Return Loss (-20 dBm Pin)

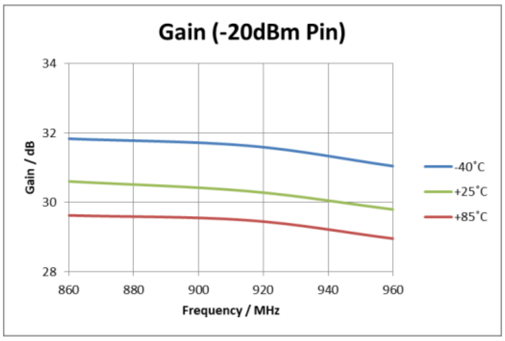


Figure 16: Gain (-20 dBm Pin)

Ta = 25˚C, Vbias = 3.3 V, Vctrl = 3.3 V, Zo = 50 Ω

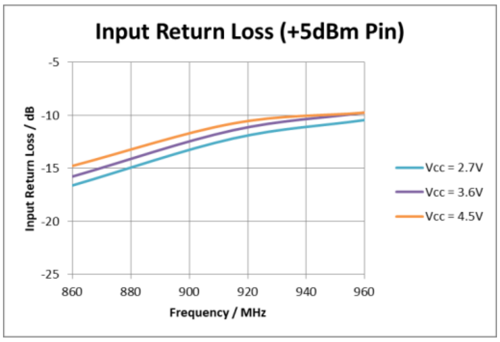


Figure 13: Input Return Loss (+5 dBm Pin)

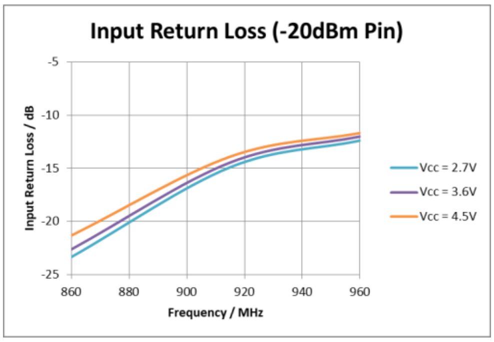


Figure 15: Input Return Loss (-20 dBm Pin)

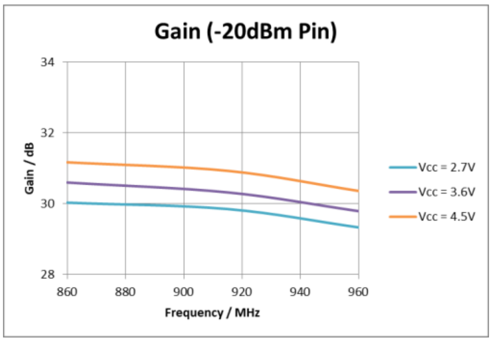


Figure 17: Gain (-20 dBm Pin)

Test conditions unless otherwise noted:-

Vcc = 3.6 V, Vbias = 3.3 V, Vctrl = 3.3 V, Zo = 50 Ω

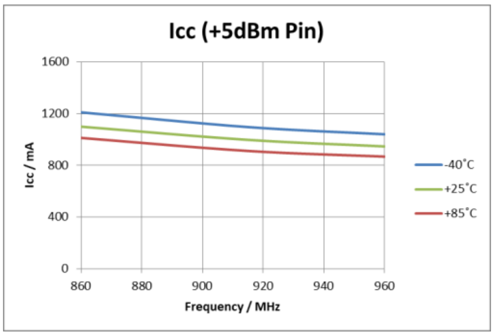


Figure 18: Icc (+5 dBm Pin)

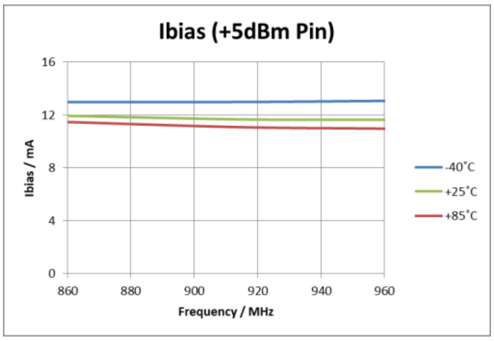


Figure 20: Ibias (+5 dBm Pin)

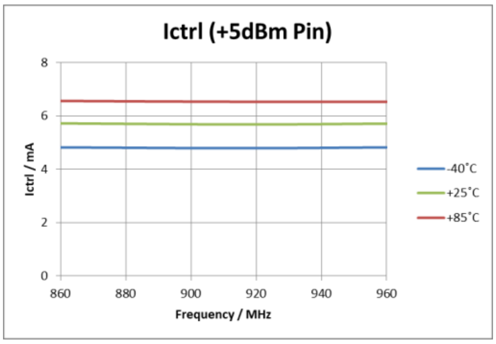


Figure 22: Ictrl (+5 dBm Pin)

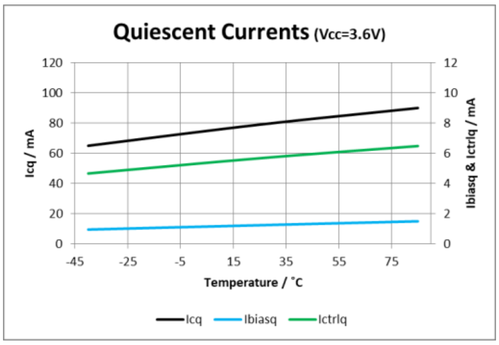


Figure 24: Quiescent Currents

Ta = 25˚C, Vbias = 3.3 V, Vctrl = 3.3 V, Zo = 50 Ω

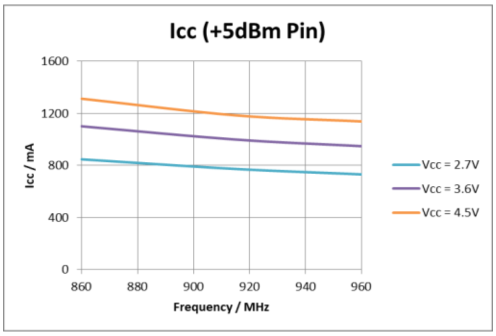


Figure 19: Icc (+5 dBm Pin)

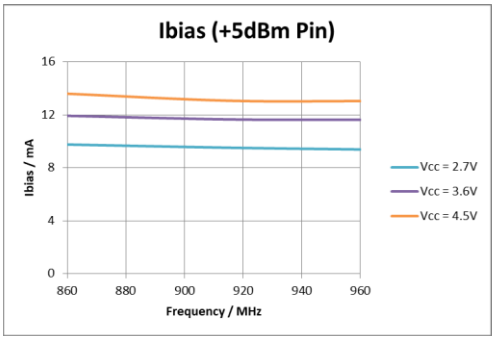


Figure 21: Ibias (+5 dBm Pin)

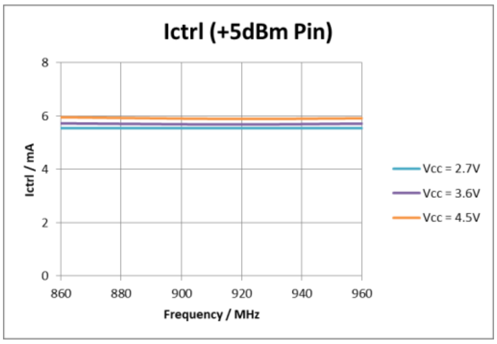


Figure 23: Ictrl (+5 dBm Pin)

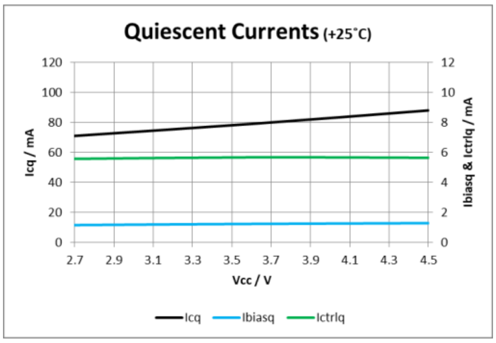


Figure 25: Quiescent Currents

Test conditions unless otherwise noted:-

Vcc = 3.6 V, Vbias = 3.3 V, Vctrl = 3.3 V, Ta = 25˚C, Pin = -20 dBm, Zo = 50 Ω

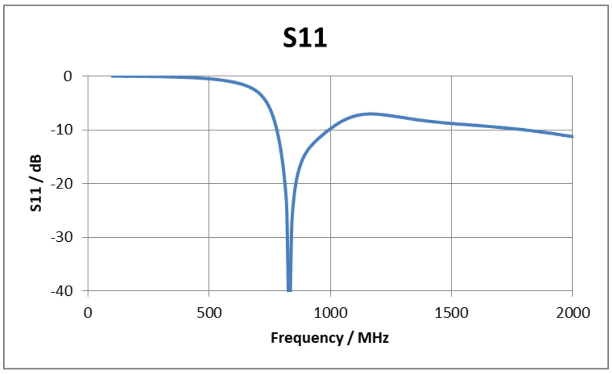


Figure 26: Input Return Loss (S11)

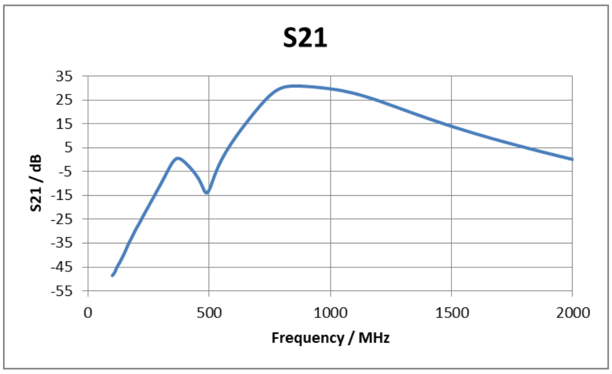


Figure 27: Small Signal Gain (S21)

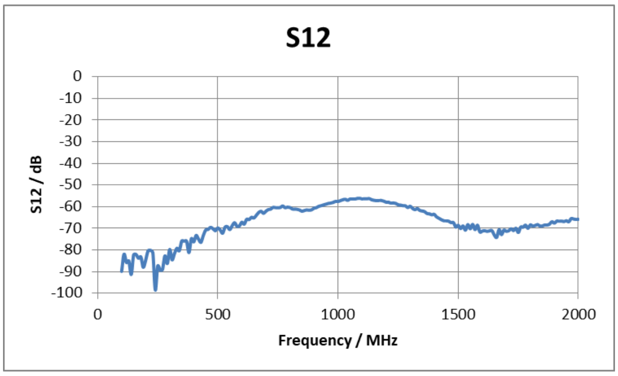


Figure 28: Reverse Isolation (S12)

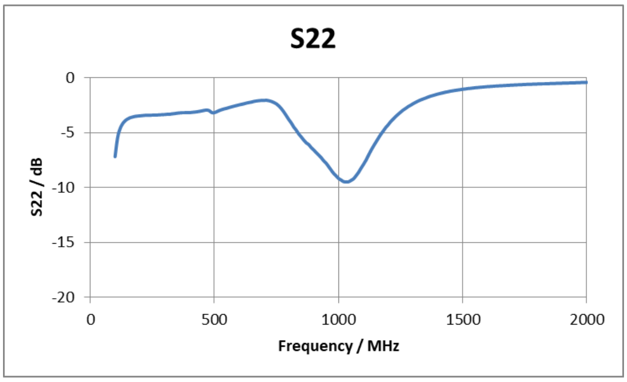


Figure 29: Output Return Loss (S22)

Application Information

Schematic Diagram

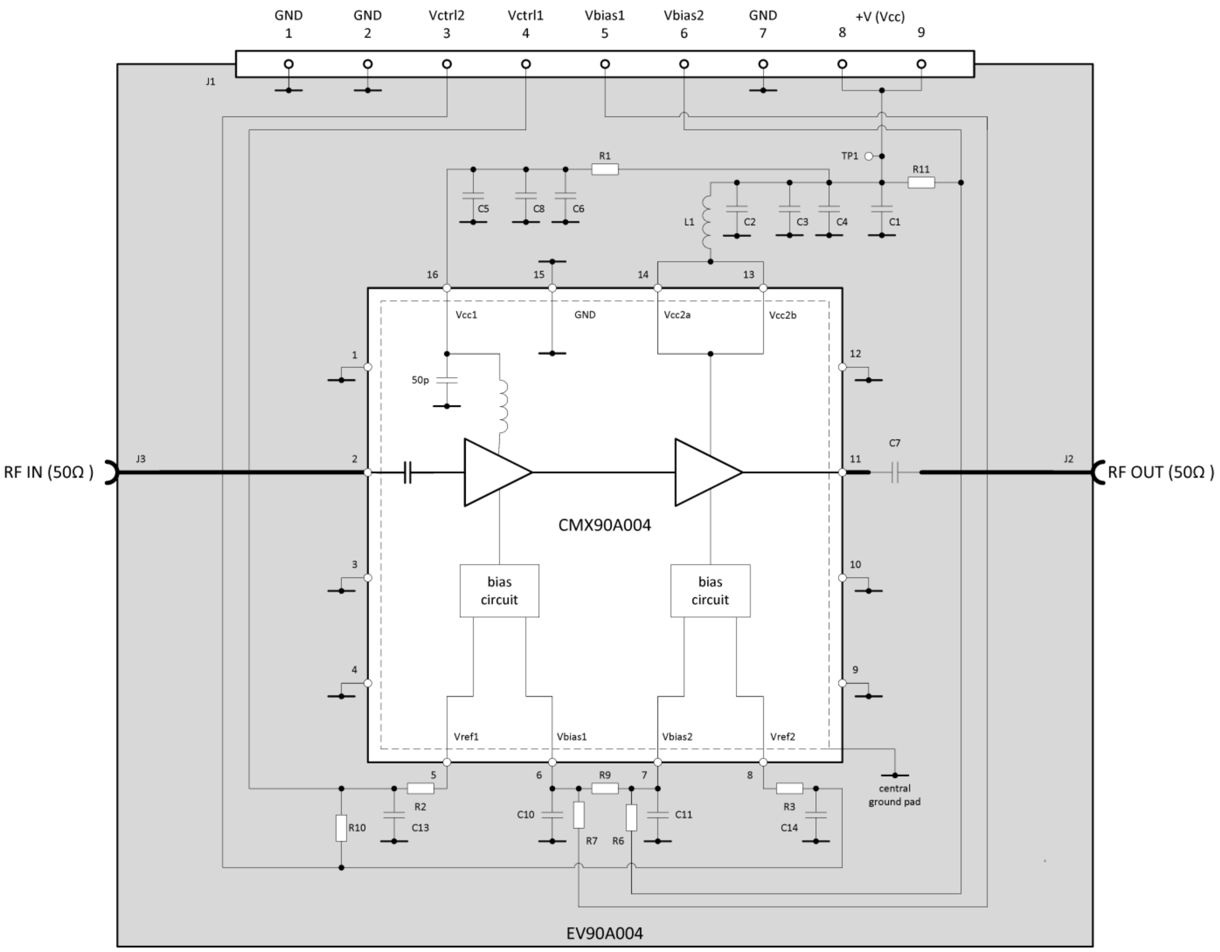


Figure 30: EV90A004 Schematic

Bill Of Materials (BOM)

Reference Designator	Value	Size	Description
C1	10 uF	0603	10V, +/-10 %
C2	47 pF	0402	25V, +/-5 %
C3	10 nF	0402	16V, +/-10 %
C4	DNF		
C5	DNF		
C6	DNF		
C7	100 pF	0402	25V, +/-5%
C8	10 nF	0402	16V, +/-10 %
C10	1 uF	0402	10V, +/-10%
C11	DNF		
C13	10 nF	0402	16V, +/-10 %
C14	10 nF	0402	16V, +/-10 %
L1	33 nH	0603	5 %
R1	0 R	0603	0.063 W, +/-1%
R2	270 R	0603	0.063 W, +/-1%
R3	270 R	0603	0.063 W, +/-1%
R6	DNF		
R7	0R	0603	0.063 W, +/-1%
R9	0R	0603	0.063 W, +/-1%
R10	DNF		
R11	DNF		

Notes

- DNF = Do not fit component
- The recommended manufacturer for the inductor (L1) is Coilcraft, manufacturer part # 0603AF-33NXJE.

PCB Layout

Careful layout of the printed circuit board (PCB) is essential for optimum RF and thermal performance. The recommended layout, including ground via pattern underneath the device, may be taken from the evaluation board (Part Number EV90A004). See following section for recommendations on best thermal design.

The PCB consists of four layer FR-4 with a total thickness of 1.6 mm (Figure 31) and the EV90A004 PCB (Figure 32) is 50 mm x 50 mm. The microstrip RF input and output width is 0.35 mm.

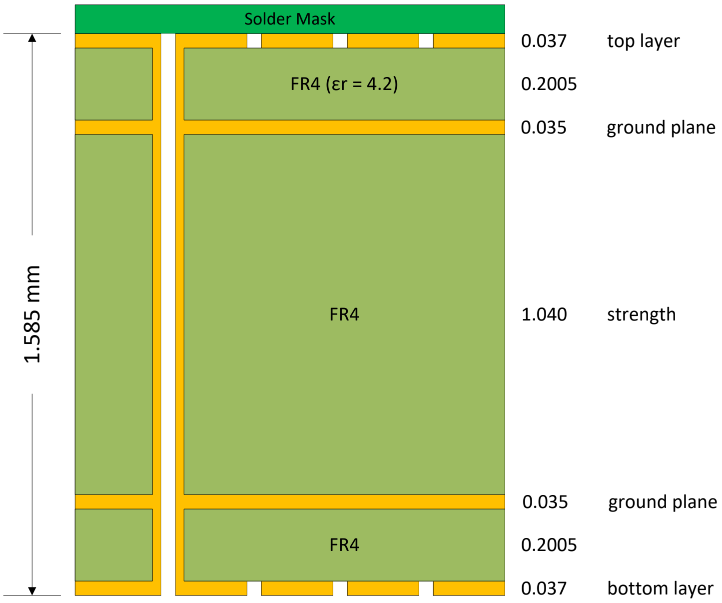


Figure 31: EV90A004 PCB Layer Stack

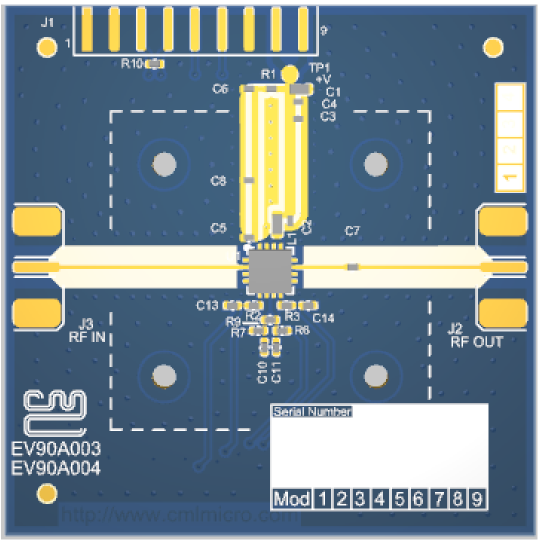


Figure 32: EV90A004 PCB Top Layer View

Thermal Design

The primary RF/DC ground and thermal path is via the exposed die pad on the backside of the package, which must be connected to the PCB ground plane. An array of plated through-hole vias directly underneath the die pad area is essential to conduct heat away and minimise ground inductance. A typical solution should have 9 grounding vias connecting the top layer to the bottom layer, with inner diameter of 0.2 mm (and 0.025 mm plating) on 0.875 mm grid pattern. The vias do not need to be filled. The PCB layout should provide a thermal radiator appropriate for the intended operation, adding as much copper to inner and outer layers as possible to avoid excessive junction temperature.

Device junction temperature (Tj) can be calculated using Tj = Tc + (Pdiss x Rjc) where Pdiss = Pdc + Pin - Pout and Tc is the case temperature on the backside of the package (die pad) in contact with the PCB.

A heatsink should be used if the thermal performance of the PCB layout is not adequate and particularly if the user is running the device continuous at Psat. The heatsink should be attached to the rear of the PCB using mounting screws positioned close to the device to ensure good contact with the ground via pattern. The backside of the PCB is clear of solder resist to enable a heatsink to be applied.

Vref Pins

The quiescent bias current of each stage is proportional to the current into the associated Vref pin. This current is set by a series resistor from the Vctrl regulated supply. These resistors are 270 Ω on the EV90A004, resulting in the following currents:

Current into Vref1 = (Vctrl1 – 2.40) / (270 + 54.0) = 2.78mA (with Vctrl1 = 3.3V)
Current into Vref2 = (Vctrl2 – 2.40) / (270 + 42.5) = 2.88mA (with Vctrl2 = 3.3V)

These bias points have been selected for optimum PA efficiency. It is possible to achieve these same currents from higher or lower Vctrl supplies by appropriate selection of the series resistors. To ensure correct bias circuit operation the current into either Vref1 or Vref2 should not exceed 5mA.

The device can be placed into standby mode when not in use by setting Vctrl low (<1.5V) to disable the bias circuits. Vctrl can also be used to ramp the CMX90A004 output power up or down to support burst signals and TDD systems. By varying Vref between 1.5 V and 2.5 V (typ.) the output power can be adjusted by more than >65 dB (Figure 33). Controlling each Vctrl input separately contributes approximately half of the total control range.

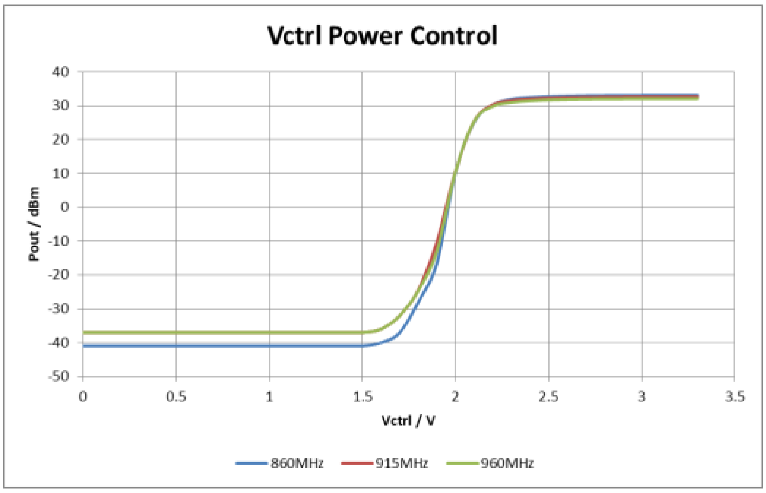


Figure 33: Vctrl Power Control

Vbias Pins

The Vbias pins provide the supply to the bias circuits and the associated base current to the two amplifier stages.

To consolidate power supplies the Vbias pins can be connected to Vcc without affecting the performance of the device. The output power performance with Vbias connected to Vcc is compared with Vbias connected to a fixed 3.3V supply.

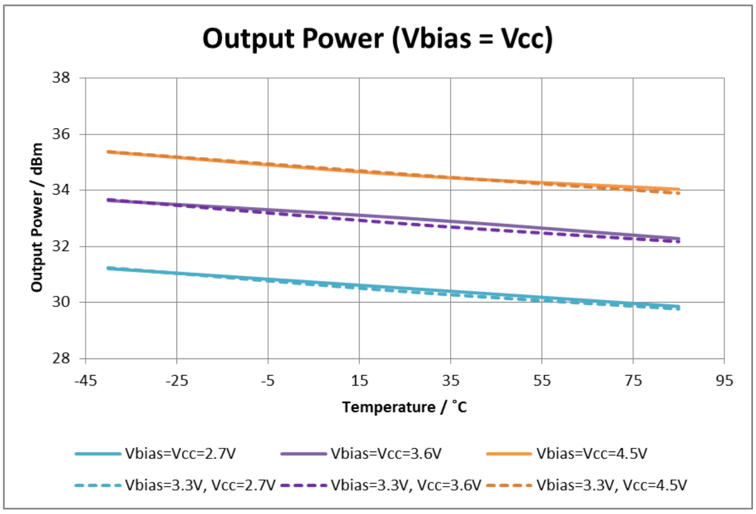


Figure 34: Output Power (Vbias = Vcc)

Evaluation Board and Bias Procedure

Ensure an adequately rated attenuator is placed between the output of the amplifier (RFout) and 50 Ω RF test equipment. The amplifier RFin should be connected to a signal generator with RF off. A dual power supply will be needed, with output of +3.6 V @ 2 A for the collector voltage (Vcc) and +3.3 V @ 100 mA for the bias circuitry (Vbias and Vref). Use good quality cables to minimise any voltage drop between the PSU and evaluation board. Connect the power supply with RF off and ensure that the evaluation board consumes the correct quiescent current (Icq). Although it is good practice to enable the Vcc supply before the bias circuitry, in general, power supply sequencing is not necessary. If the quiescent current is correct, enable the RF signal with a low level RFin = -30 dBm to begin with to ensure the device is not overdriven. Ensure the test signal is within the recommended frequency range of the device and that the output signal measured on the test equipment complies with small signal gain, before continuing with any further tests.

Standard power supply connections.

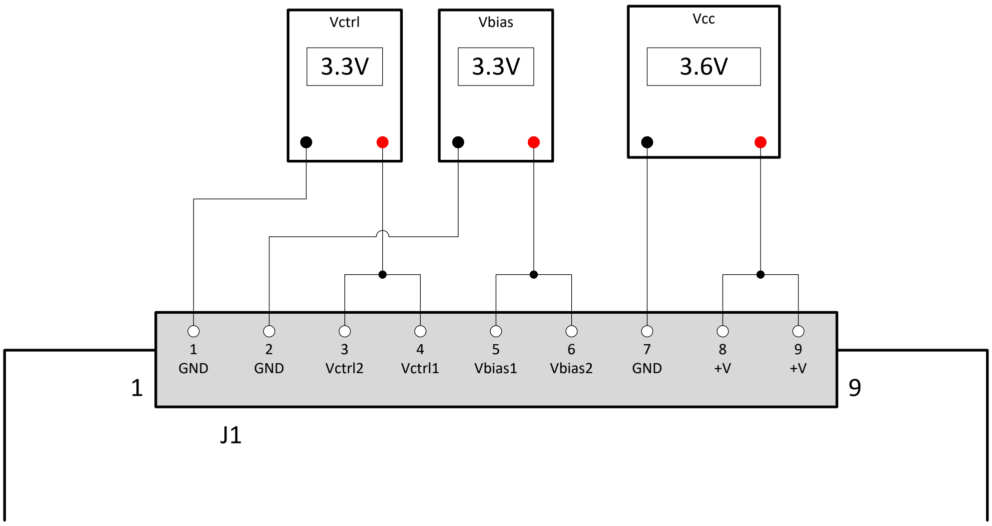


Figure 35: Standard Power Supply Connections

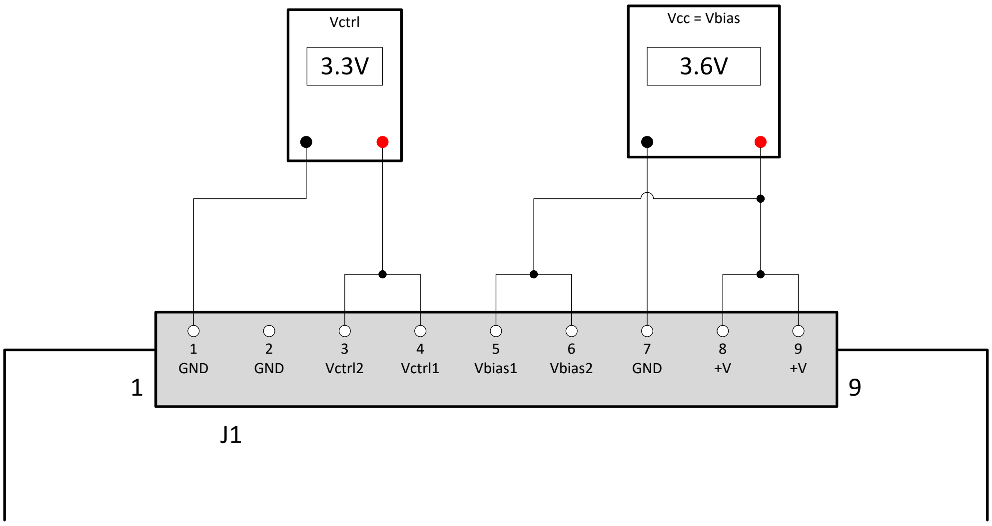


Figure 36: Alternative Power Supply Connections with Vbias = Vcc

Ruggedness

To prevent possible damage to the device, care should be taken to ensure that the VSWR of the load that the CMX90A004 is working into does not exceed the limits in the Electrical Specification. The following table shows the equivalent minimum return loss that the load should present to the CMX90A004 depending on the supply voltage applied.

Vcc	VSWR Limit	Return Loss
2.7 – 4.0 V	5:1	>3.5 dB
4.0 – 4.5 V	3:1	>6.0 dB

The maximum possible supply voltage should be taken into account when designing with the CMX90A004 PA. This is particularly important when Vcc is derived from a battery that can have a higher voltage than nominal when fully charged, for example a 3.6 V Li-ion battery at full charge is usually at 4.2 V.

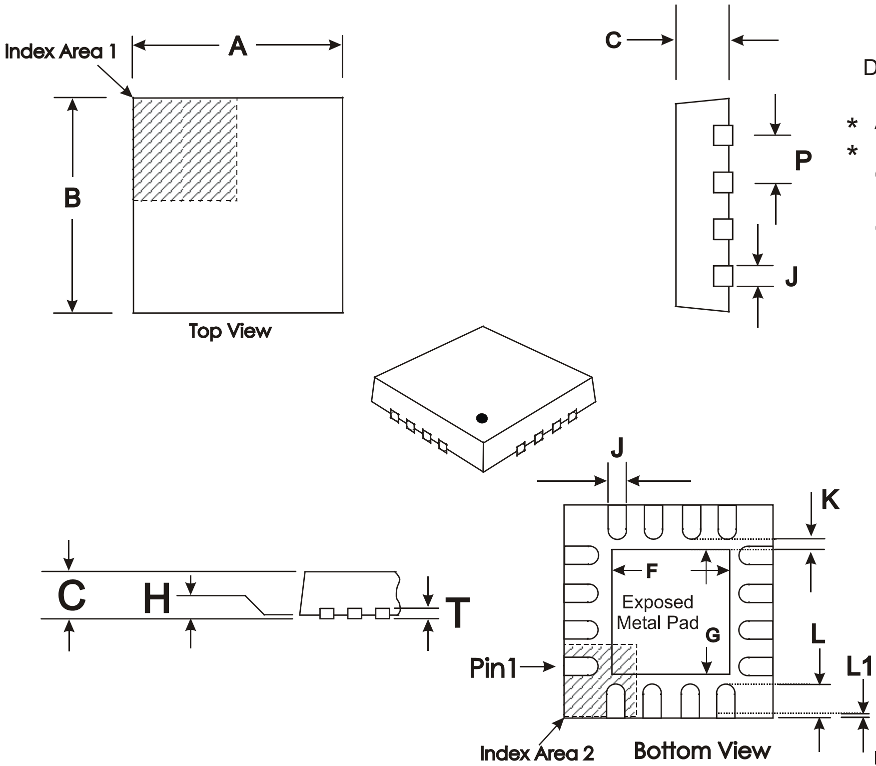
A typical transmit system will have filtering, transmit/receive switching and antenna matching between the PA and the antenna. These all need to be designed carefully to ensure a good 50 Ω match is presented to the PA that is above the minimum return loss limits over the whole operating frequency range.

External effects on the antenna impedance should also be taken into account. Proximity to other objects and surfaces can change the antenna impedance significantly, resulting in the return loss presented to the PA falling below the limit and therefore subsequent damage to the PA.

If there is an external antenna connector on the equipment, it should be assumed that the wrong antenna might get connected or that the transmitter may be operated with no antenna connected. To avoid the resulting high VSWR damaging the PA additional protection such as a circulator may be necessary.

Package Outline

16-lead 4x4mm VQFN Package (Q7)

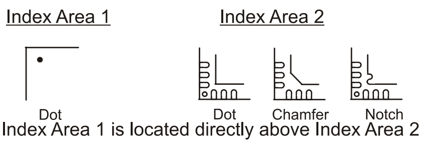


DIM.	MIN.	TYP.	MAX.
* A		4.00 BSC	
* B		4.00 BSC	
C	0.80	0.90	1.00
F	2.55		2.80
G	2.55		2.80
H	0.00		0.05
J	0.22	0.30	0.35
K	0.20		
L	0.30		0.50
L1	0		0.15
P		0.65	
T		0.20	

NOTE :

A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees

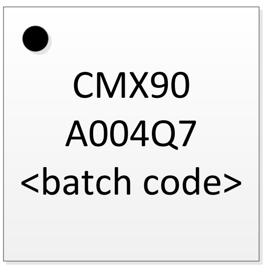


Index Area 1 is located directly above Index Area 2

Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.
L minus L1 to be equal to, or greater than 0.3mm
The underside of the package has an exposed metal pad which should ideally be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

Package Marking

Pin 1 indicator (dot) and 3 rows of text for device identification.



Line 1: CMX90 SμRF series

Line 2: 4-character part code and 2-character package code

Line 3: Batch code

Revision History

Issue	Description	Date
2	Change of product codes for ordering	September 2022
1	First public release	March 2021

Contact Information

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