CML Microcircuits

COMMUNICATION SEMICONDUCTORS

CMX7131/CMX7141
Digital PMR Processor
NXDN™ Operation

D/7141_FI-3.x/7.1 December 2015

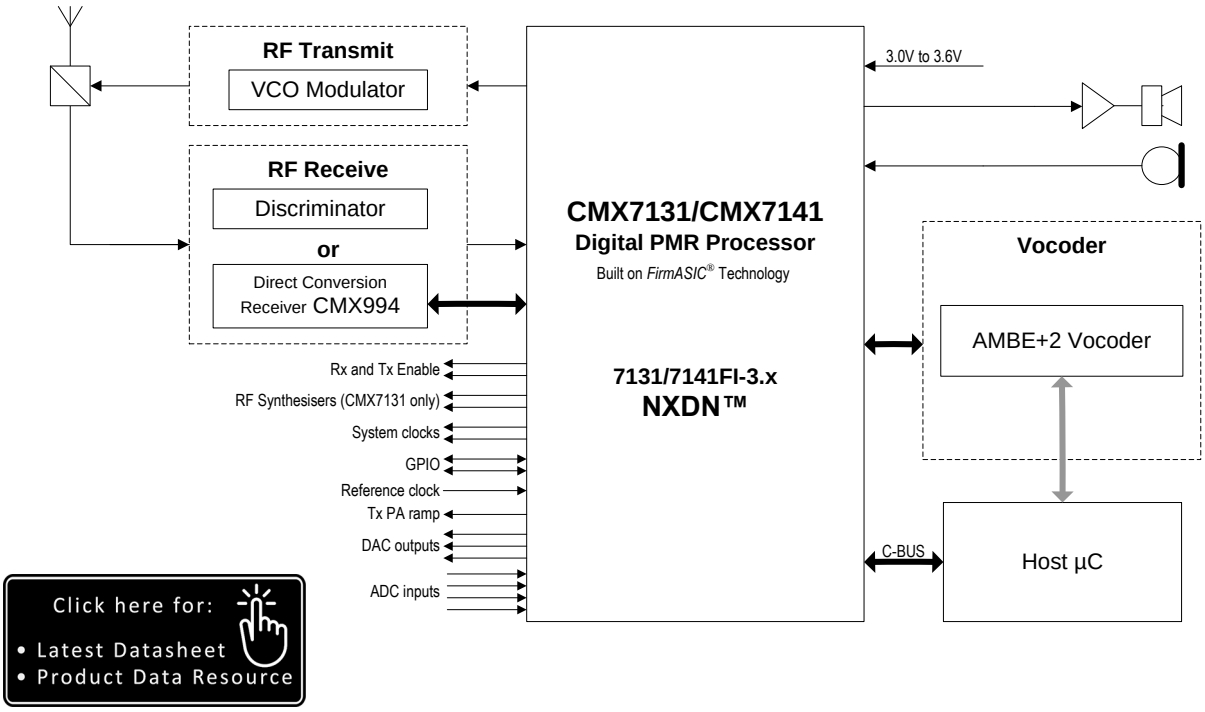
DATASHEET

Advance Information

7131/7141FI-3.x: NXDN™ 4-FSK Baseband Data Processor with Auxiliary System Clocks, ADCs and DACs

Features

- 4-FSK Modem
  - 4.8 or 9.6 kbps Data Rate
  - Soft-decision Data Output Option
  - AFSD (Automated Frame Sync Detection)
- Vocoder Connectivity
  - AMBE+2 Vocoder, e.g. AMBE-3000
- Tx Outputs for Two-point or I/Q Modulation
- Rx Inputs for CMX994 Direct Conversion Receiver
- NXDN™ Half rate and Full rate support
- NXDN™ Conventional and Class-D trunking support
- Tx Sequencer reduces host timing constraints
- Two RF Synthesisers (CMX7131 only)
- Four Auxiliary ADCs (4 Multiplexed Inputs)
- Four Auxiliary DACs
- Two Auxiliary System Clock Outputs
- Flexible Powersave Modes
- Available in LQFP or VQFN Packages
- Low-power (3.0 to 3.6V) Operation
- C-BUS Serial Interface to Host µController



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Datasheet | User Manual

1 Brief Description

The CMX7131/CMX7141 when loaded with 7131/7141FI-3.x implements a half-duplex 4-FSK modem and a large proportion of the NXDN Air Interface (physical) layer and Data Link layer. In conjunction with a suitable host, voice coder and limiter/discriminator or CMX994 Direct Conversion (I/Q) Receiver based RF transceiver, a compact, low cost, low power digital PMR radio conforming to the NXDN™ standard can be realised. The 7131/7141FI-3.x has two receiver interface modes: Limiter/Discriminator (LD) mode is selected by default for conventional limiter/discriminator receivers; I/Q mode is tailored for operation with the CMX994 Direct Conversion Receiver IC. Dual mode, analogue/NXDN™ operation can also be achieved by alternatively loading either 7031/7041FI-1 or 7131/7141FI-8 analogue FM Function Images™.

Support for both half-rate and full-rate (4800 bps and 9600 bps) modem modes are provided, along with Conventional and Class-D trunking protocol support (Note that Vocoder support is limited to EHR mode in all modes).

The embedded functionality of the CMX7131/CMX7141 allows managing voice and data systems autonomously. Host microcontroller interactions are minimised, enabling the lowest operating power and therefore the longest battery life for a NXDN radio. The CMX7131/CMX7141 can also provide audio codec functionality for vocoders under direct host control.

The device utilises CML's proprietary *FirmASIC*® component technology. On-chip sub-systems are configured by a Function Image™: this is a data file that is uploaded during device initialisation and defines the device's function and feature set. The Function Image™ can be loaded automatically from an external serial memory or host µController over the built-in C-BUS serial interface. The device's functions and features may be enhanced by subsequent Function Image™ releases, facilitating in-the-field upgrades. This document refers specifically to the features provided by 7131/7141 FI-3.x.

Other features include two auxiliary ADCs with four selectable inputs and four auxiliary DAC interfaces (with an optional RAMDAC on the first DAC output, to facilitate transmitter power ramping). The CMX7131 features two on-chip RF synthesisers, with easy Rx/Tx frequency changeover.

The CMX7141 is identical in functionality to the CMX7131, with the exception that the two on-chip RF synthesisers have been deleted, which enables it to be supplied in a smaller package. This document refers to both parts generically as the CMX7141, unless otherwise stated.

The device has flexible powersaving modes and is available in both LQFP and VQFN packages.

Note that text shown in pale grey indicates features that may be supported in future versions of the Function Image™.

This Datasheet is the first part of a two-part document comprising Datasheet and User Manual: the User Manual can be obtained from the CML Technical Portal by registering your interest in this product with your local CML representative.

This datasheet is the first part of a two-part document

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Information in this datasheet should not be relied upon for final product design. It is always recommended that you check for the latest product datasheet version from the CML website: [www.cmlmicro.com].

History

Version	Changes	Date
7.1	• References to full rate (9600bps for 12.5kHz systems) added throughout entire Datasheet • Rx with Powersave mode changed to Rx with CMX994 Powersave mode throughout entire document • Section 6.5.11: Tx Sequencer functionality now included • Section 6.5.17 and 6.5.18 enhanced to clarify operation with CMX994 • Section 6.8: added text to describe the ability to set TXENA and RXENA pins active high via register $A7 • Section 8.1.3: Register $A7, bit 1 now inverts logic levels of RxENA and TxENA • Section 8.1.5: entire bit table restructured to improve clarity • Section 8.1.21: $C0, b4, now reserved. • Section 8.1.24: $C3 renamed from Vocoder Analogue Gain to Analogue Gain – in this section and throughout entire document • Section 8.1.24: added table to clarify setting of MOD fine gain. • Section 8.1.26: IRQ Status ($C6) register – bit 13 now enables powersave exit functionality • Section 8.1.33: AuxConfig ($CD) register description restructured to improve clarity. Settings for squelch removed • Section 8.2.1: Program Block 0 description restructured to improve clarity. • Added Section 8.3 (additional features for use with CMX7241/CMX7341 platform) • Section 9, Function Image Updates • NXDN™ Class-D trunking support added (Class D scheduled for a future release and therefore shown in grey)	December 2015
7	• Reserved for internal use only	October 2015
6	• Vocoder-related content was clarified throughout the document. • AMBE+2 now described as the default decoder throughout entire document • Section 6.5.11: Tx Sequencer description revised • Section 6.5.15, Figure 21: new graph replaces table • Section 8.1.24 - $C3 register description revised • Section 8.2.3 – P2.0 description now describes Rx audio pass-through operation (b3) • Section 8.2.3, Figure 33: new graph replaces table • Section 9, Function Image Updates	April 2014
5	• Completely revised for FI-3.1 and NXDN operation • Updated RAMDAC and tone generator descriptions • Added RSSI - signal strength graph • Expanded description of Fine Level adjustment of outputs • Various typographical and editorial changes and update to version history.	Sep 2013

4	• Correction to FS2 detector operation in section 6.3.5 • FS1 and FS2 bits changed to a single FS Det bit in sections 6.3.5, 10.1.25 and 10.1.32 • Additional RAMDAC information in section 10.1.4 • Corrected b3-0 order in Table 4 and section 10.1.22 • Sync task removed from Table 5, section 10.1.22 and section 10.1.28 • Added information about Abort/Reset in section 7.5.7	Sep 2012
3	• Clarification of BOOTEN states and corrections to RF Synthesiser specification • Correction to SPI bus Chip Select pin definition.	Sep 2011
2	• Third party vocoder added and diagrams updated • CMX7131 features added • C-BUS signal names standardised and reset conditions added	July 2010
1	• Original document, prepared for internal use.	Mar 2009

This is Advance Information; changes and additions may be made to this specification. Parameters marked TBD or left blank will be included in later issues. Items that are highlighted or greyed out should be ignored. These will be clarified in later issues of this document.
Information in this datasheet should not be relied upon for final product design.

2 Block Diagram

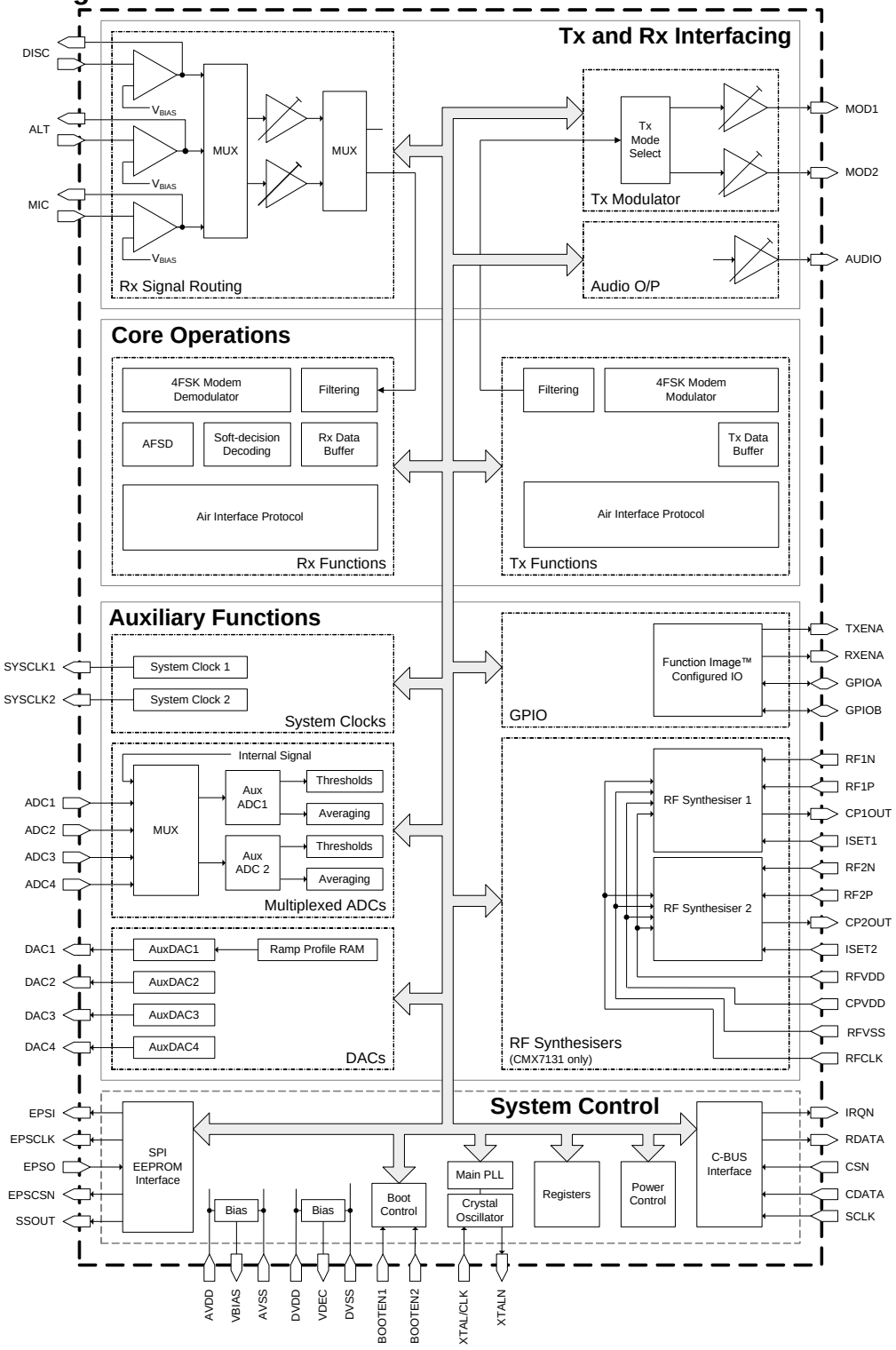


Figure 1 CMX7141 Block Diagram

3 Signal List

CMX7131 64-pin Q1/L9	CMX7141 48-pin Q3/L4	Pin Name	Type	Description
1	**8**	IRQN	OP	C-BUS: A 'wire-ORable' output for connection to the Interrupt Request input of the host. Pulled down to DV_{SS} when active and is high impedance when inactive. An external pull-up resistor (R1) is required.
2	-	RF1N	IP	RF Synthesiser 1 negative input
3	-	RF1P	IP	RF Synthesiser 1 positive input
4	-	RFVSS	PWR	The negative supply rail (ground) for RF Synthesiser 1
5	-	CP1OUT	OP	RF Synthesiser 1 Charge Pump output
6	-	ISET1	IP	RF Synthesiser 1 Charge Pump Current Set input
7	-	RFVDD	PWR	The 2.5V positive supply rail for both RF Synthesisers. This should be decoupled to RFV_{SS} by a capacitor mounted close to the device pins.
8	-	RF2N	IP	RF Synthesiser 2 negative input
9	-	RF2P	IP	RF Synthesiser 2 positive input
10	-	RFVSS	PWR	The negative supply rail (ground) for RF Synthesiser 2
11	-	CP2OUT	OP	RF Synthesiser 2 Charge Pump output
12	-	ISET2	IP	RF Synthesiser 2 Charge Pump Current Set input
13	-	CPVDD	PWR	The 3.3V positive supply rail for the RF Synthesiser charge pumps. This should be decoupled to RFV_{SS} by a capacitor mounted close to the device pins.
14	-	RFCLK	IP	RF Clock Input (common to both RF Synthesisers)[1]
15	**11**	GPIOA	OP	General purpose I/O pin
16	**12**	GPIOB	OP	General purpose I/O pin
17	-	-	NC	Reserved – do not connect this pin
18	**9**	VDEC	PWR	Internally generated 2.5V digital supply voltage. Must be decoupled to DV_{SS} by capacitors mounted close to the device pins. No other connections allowed, except for optional connection to RFV_{DD}.
19	**10**	RXENA	OP	Rx Enable – active low when in Rx mode ($C1:b0 = 1)
20	**13**	SYSCLK1	OP	Synthesised Digital System Clock Output 1
21	**14**	DVSS	PWR	Digital ground
22	-	-	NC	Reserved – do not connect this pin
23	**15**	TXENA	OP	Tx Enable – active low when in Tx mode ($C1:b1 = 1)
24	**16**	DISC	IP	Discriminator inverting input
25	**17**	DISCFB	OP	Discriminator input amplifier feedback

[1] To minimise crosstalk, this signal should be connected to the same clock source as XTAL/CLK input.

CMX7131 64-pin Q1/L9	CMX7141 48-pin Q3/L4	Pin Name	Type	Description	
26	**18**	ALT	IP	Alternate inverting input	
27	**19**	ALTFB	OP	Alternate input amplifier feedback	
28	**20**	MICFB	OP	Microphone input amplifier feedback	
29	**21**	MIC	IP	Microphone inverting input	
30	**22**	AVSS	PWR	Analogue ground	
31	**23**	MOD1	OP	Modulator 1 output	
32	**24**	MOD2	OP	Modulator 2 output	
33	**25**	VBIAS	OP	Internally generated bias voltage of about $AV_{DD}/2$, except when the device is in 'Powersave' mode when V_{BIAS} will discharge to AV_{SS}. Must be decoupled to AV_{SS} by a capacitor mounted close to the device pins. No other connections allowed.	
34	**26**	AUDIO	OP	Audio Output in SPI-Codec mode	
35	**27**	ADC1	IP	Auxiliary ADC input 1	Each of the two ADC blocks can select its input signal from any one of these input pins, or from the MIC, ALT or DISC input pins. See section 8.1.3 for details.
36	**28**	ADC2	IP	Auxiliary ADC input 2	
37	**29**	ADC3	IP	Auxiliary ADC input 3	
38	**30**	ADC4	IP	Auxiliary ADC input 4	
39	**31**	AVDD	PWR	Analogue +3.3V supply rail. Levels and thresholds within the device are proportional to this voltage. This pin should be decoupled to AV_{SS} by capacitors mounted close to the device pins.	
40	**32**	DAC1	OP	Auxiliary DAC output 1/RAMDAC	
41	**33**	DAC2	OP	Auxiliary DAC output 2	
42	**34**	AVSS	PWR	Analogue ground	
43	**35**	DAC3	OP	Auxiliary DAC output 3	
44	**36**	DAC4	OP	Auxiliary DAC output 4	
-	**37**	DVSS	PWR	Digital ground	
45	**38**	VDEC	PWR	Internally generated 2.5V supply voltage. Must be decoupled to DV_{SS} by capacitors mounted close to the device pins. No other connections allowed, except for the optional connection to RFV_{DD}.	
46	**39**	XTAL/CLK	IP	Input from the external clock source or Xtal	
47	**40**	XTALN	OP	The output of the on-chip Xtal oscillator inverter. NC if external clock used.	
48	**41**	DVDD	PWR	Digital +3.3V supply rail. This pin should be decoupled to DV_{SS} by capacitors mounted close to the device pins.	
49	**42**	CDATA	IP	C-BUS Command Data: Serial data input from the µC	
50	**43**	RDATA	TS OP	C-BUS Reply Data: A 3-state C-BUS serial data output to the µC. This output is high impedance when not sending data to the µC.	

CMX7131 64-pin Q1/L9	CMX7141 48-pin Q3/L4	Pin Name	Type	Description
51	-	-	NC	Reserved – do not connect this pin
53	**44**	SSOUT	OP	SPI bus Chip Select/Frame Sync
52	**45**	DVSS	PWR	Digital ground
54	**46**	SCLK	IP	C-BUS Serial Clock: The C-BUS serial clock input from the µC
55	**47**	SYSCLK2	OP	Synthesised Digital System Clock Output 2
56	**48**	CSN	IP	C-BUS Chip Select: The C-BUS chip select input from the µC - there is no internal pullup on this input
57	-	-	NC	Reserved – do not connect this pin
58	**1**	EPSI	OP	Serial Memory Interface: Output, SPI bus Output
59	**2**	EPSCLK	OP	Serial Memory Interface: Clock, SPI bus Clock
60	**3**	EPSO	IP+PD	Serial Memory Interface: Input, SPI bus Input
61	**4**	EPSCSN	OP	Serial Memory Interface: Chip Select
62	**5**	BOOTEN1	IP+PD	Used in conjunction with BOOTEN2 to determine the operation of the bootstrap program.
63	**6**	BOOTEN2	IP+PD	Used in conjunction with BOOTEN1 to determine the operation of the bootstrap program.
64	**7**	DVSS	PWR	Digital ground
EXPOSED METAL PAD	EXPOSED METAL PAD	SUBSTRATE	~	On this device, the central metal pad (which is exposed on Q1 and Q3 packages only) may be electrically unconnected or, alternatively, may be connected to analogue ground (AV_{SS}). **No other electrical connection is permitted.**

Colour Definitions:

= Aux SPI/C-BUS

= Host C-BUS

= Analogue Inputs/Outputs

= ADCs/DACs

Notes:

IP	=	Input (+ PU/PD = internal pullup/pulldown resistor)
OP	=	Output
BI	=	Bidirectional
TS OP	=	3-state output
PWR	=	Power connection
NC	=	No Connection - should NOT be connected to any signal.

3.1 Signal Definitions

Table 1 Definition of Power Supply and Reference Voltages

Signal Name	Pins	Usage
AV_{DD}	AVDD	Power supply for analogue circuits
DV_{DD}	DVDD	Power supply for digital circuits
V_{DEC}	VDEC	Power supply for core logic, derived from DV_{DD} by on-chip regulator
V_{BIAS}	VBIAS	Internal analogue reference level, derived from AV_{DD}
AV_{SS}	AVSS	Ground for all analogue circuits
DV_{SS}	DVSS	Ground for all digital circuits
RFV_{DD}	RFVDD	Power supply for RF circuits
RFV_{SS}	RFVSS	Ground for RF circuits
CPV_{DD}	CPVDD	Power supply for charge pump circuits

4 External Components

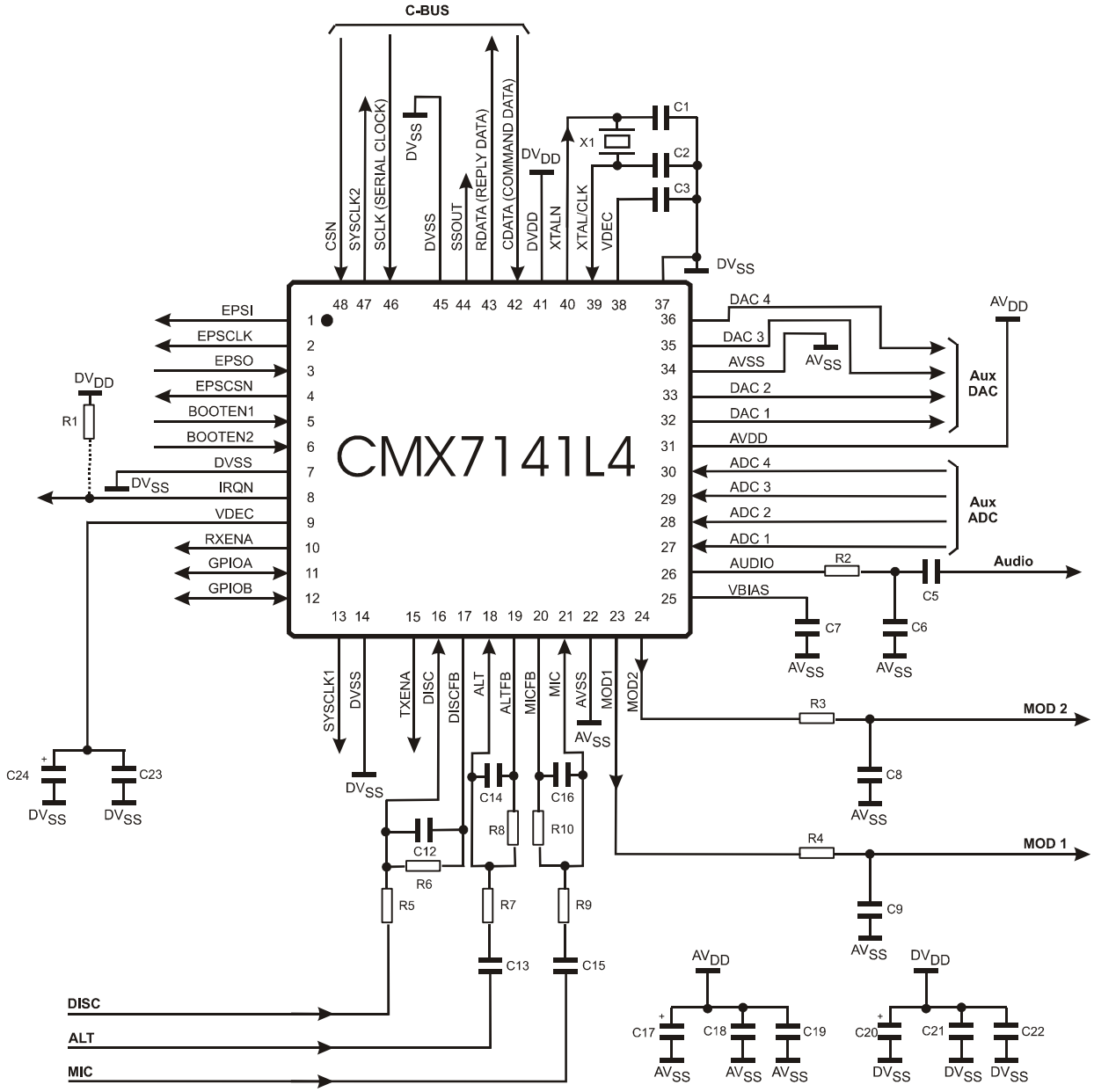


Figure 2 CMX7141 Recommended External Components

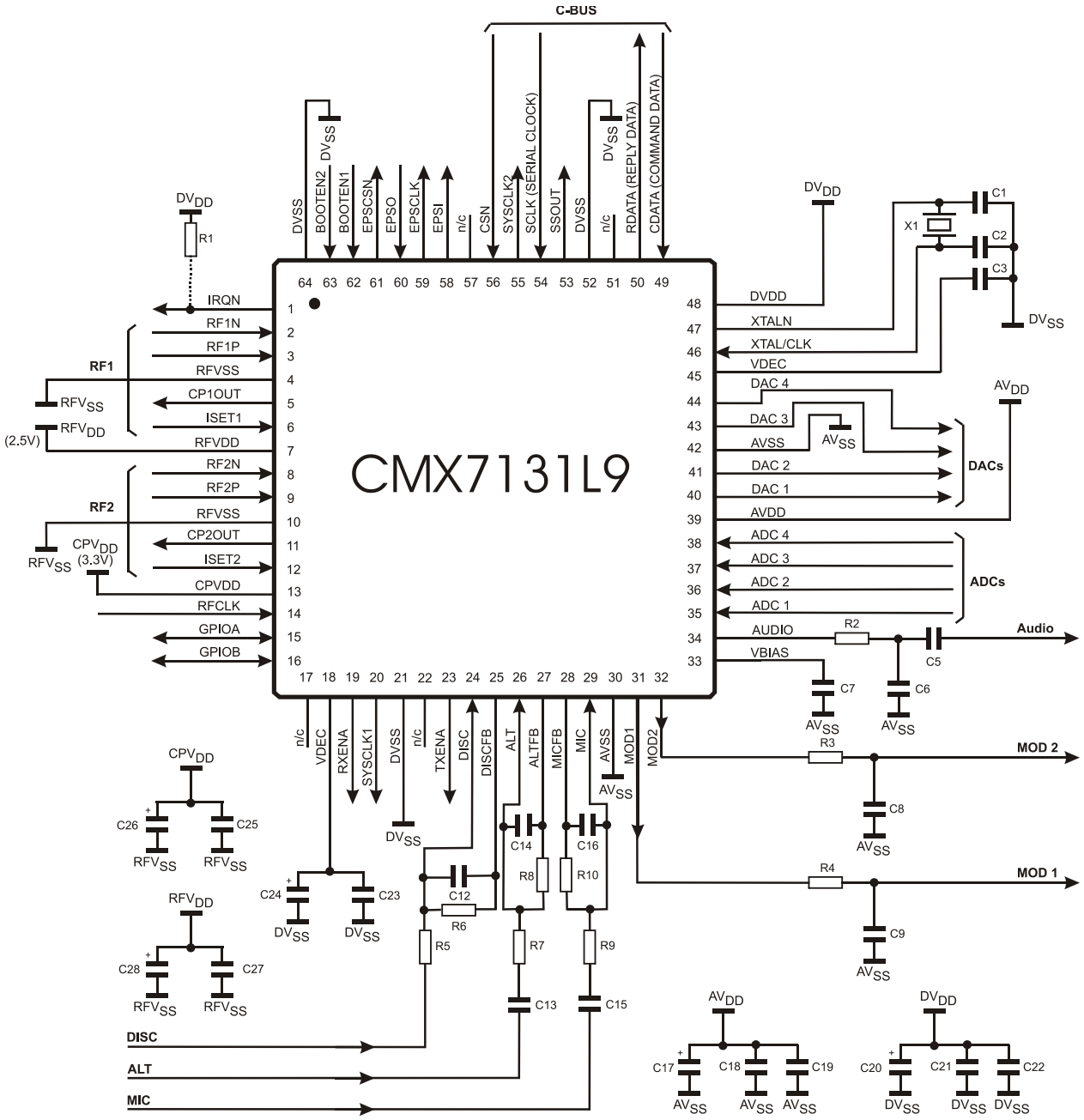


Figure 3 CMX7131 Recommended External Components

4.1 Recommended External Components

R1	100kΩ	C1	18pF	C11	*not used*	C21	10nF
R2	100kΩ	C2	18pF	C12	100pF	C22	10nF
R3	100kΩ	C3	10nF	C13	See note 5	C23	10nF
R4	100kΩ	C4	*not used*	C14	100pF	C24	10µF
R5	See note 2	C5	1nF	C15	See note 5	C25	
R6	100kΩ	C6	100pF	C16	200pF	C26	
R7	See note 3	C7	100nF	C17	10µF	C27	
R8	100kΩ	C8	100pF	C18	10nF	C28	
R9	See note 4	C9	100pF	C19	10nF	X1	6.144MHz
R10	100kΩ	C10	*not used*	C20	10µF		See note 1

Resistors ±5%, capacitors and inductors ±20% unless otherwise stated.

Notes:

1. X1 can be a crystal or an external clock generator; this will depend on the application. The tracks between the crystal and the device pins should be as short as possible to achieve maximum stability and best start up performance. By default, a 19.2MHz oscillator is assumed (in which case C1 and C2 are not required), other values could be used if the various internal clock dividers are set to appropriate values.

2. R5 should be selected to provide the desired dc gain of the discriminator input, as follows:

$$|GAIN_{DISC}| = 100k\Omega / R5$$

   The gain should be such that the resultant output at the DISCFB pin is within the DISC input signal range specified in 6.13.2. For 4-FSK modulation, this signal should be dc coupled from the limiter/discriminator output.

3. R7 should be selected to provide the desired dc gain (assuming C13 is not present) of the alternative input as follows:

$$|GAIN_{ALT}| = 100k\Omega / R7$$

   The gain should be such that the resultant output at the ALTFB pin is within the alternative input signal range specified in 6.13.

4. R9 should be selected to provide the desired dc gain (assuming C15 is not present) of the microphone input as follows:

$$|GAIN_{MIC}| = 100k\Omega / R9$$

   The gain should be such that the resultant output at the MICFB pin is within the microphone input signal range specified in 6.13.1. For optimum performance with low signal microphones, an additional external gain stage may be required.

5. C13 and C15 should be selected to maintain the lower frequency roll-off of the MIC and ALT inputs as follows:

$$C13 \geq 1.0\mu F \times |GAIN_{ALT}|$$

$$C15 \geq 30nF \times |GAIN_{MIC}|$$

6. ALT and ALTFB connections allow the user to have a second discriminator or microphone input. Component connections and values are as for the respective DISC and MIC networks. If this input is not required, the ALT pin should be connected to AV_{SS}.

7. AUDIO output is only used in this Function Image™ when SPI-Codec mode has been selected. It may also be used by analogue Function Images™ which may also be used on this device.

8. A single 10µF electrolytic capacitor (C24, fitted as shown) may be used for smoothing the power supply to both VDEC pins, providing they are connected together on the pcb with an adequate width power supply trace. Alternatively, separate smoothing capacitors should be connected to each VDEC pin. High frequency decoupling capacitors (C3 and C23) must always be fitted as close as possible to both VDEC pins.

4.2 PCB Layout Guidelines and Power Supply Decoupling

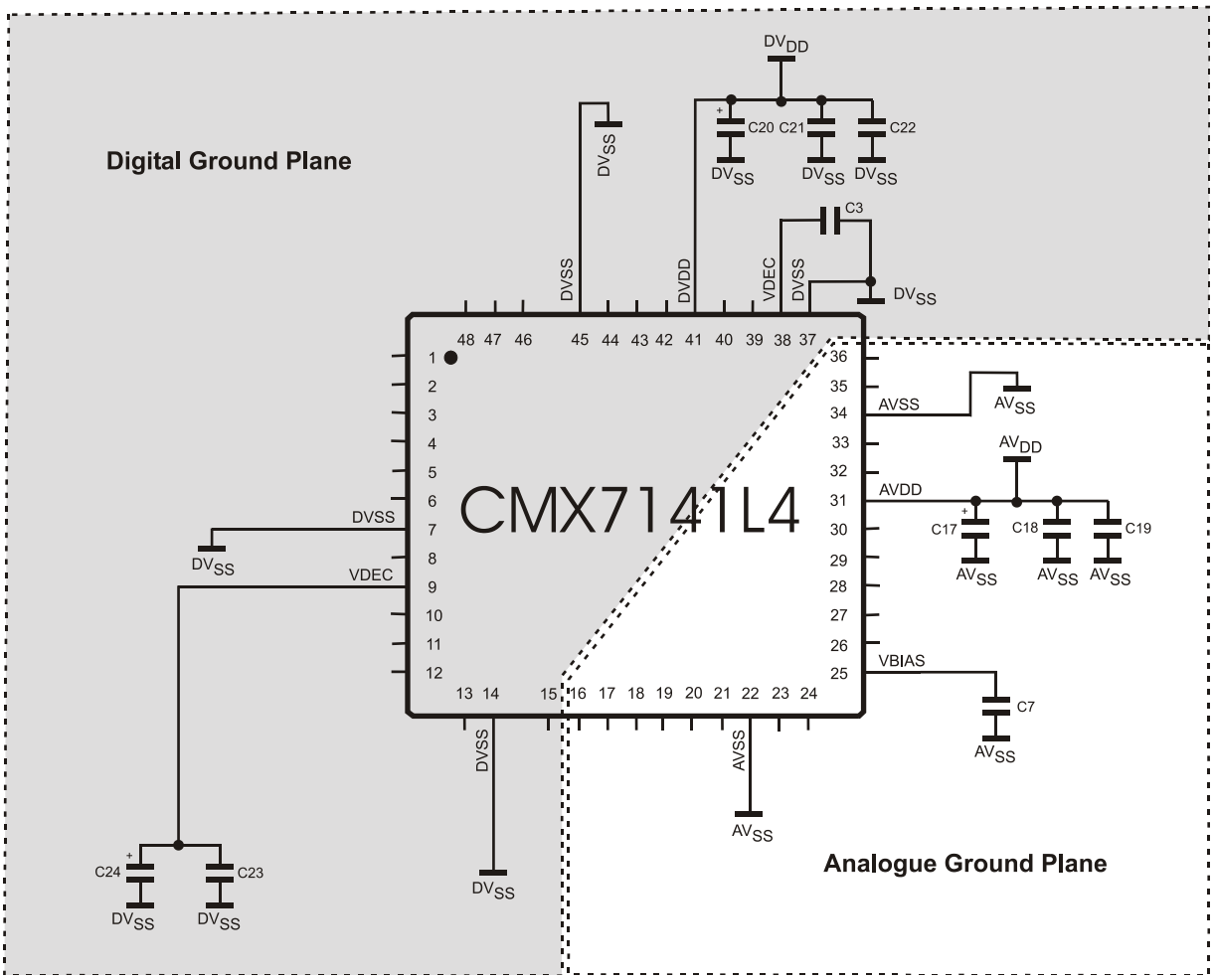


Figure 4 CMX7141 Power Supply and Decoupling

Component Values as per Figure 2

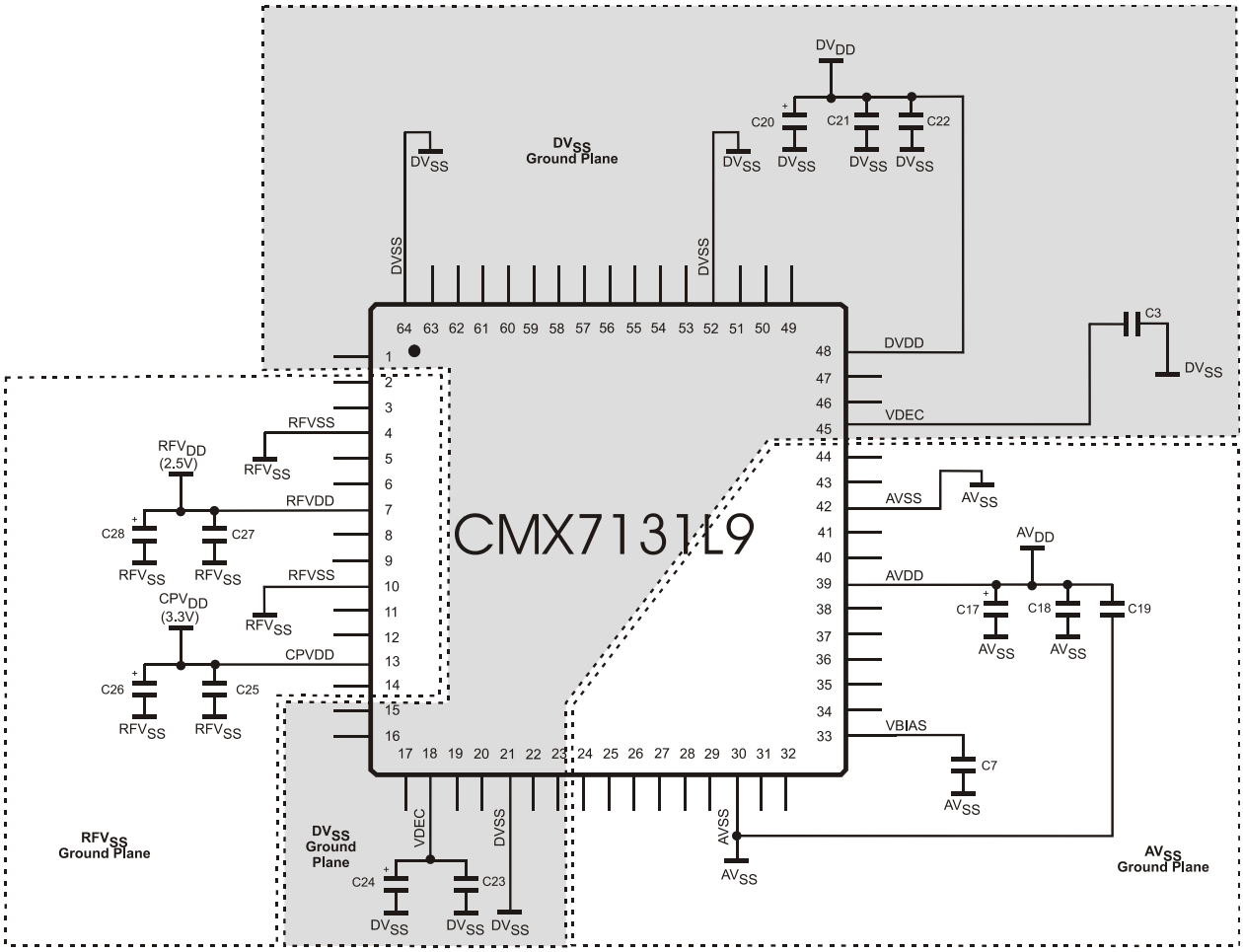


Figure 5 CMX7131 Power Supply and Decoupling

Component Values as per Figure 3

Notes:

It is important to protect the analogue pins from extraneous inband noise and to minimise the impedance between the CMX7131/CMX7141 and the supply and bias de-coupling capacitors. The de-coupling capacitors C3, C7, C18, C19, C21, C22 and C24 should be as close as possible to the CMX7131/CMX7141. It is therefore recommended that the printed circuit board is laid out with separate ground planes for the AV_{SS} and DV_{SS} supplies in the area of the CMX7131/CMX7141, with provision to make links between them, close to the CMX7131/CMX7141. Use of a multi-layer printed circuit board will facilitate the provision of ground planes on separate layers.

V_{BIAS} is used as an internal reference for detecting and generating the various analogue signals. It must be carefully decoupled, to ensure its integrity, so apart from the decoupling capacitor shown, no other loads should be connected. If V_{BIAS} needs to be used to set the discriminator mid-point reference, it should be buffered with a high input impedance buffer.

The single-ended microphone input and audio output must be ac coupled (as shown), so that their return paths can be connected to AV_{SS} without introducing dc offsets. Further buffering of the audio output is advised.

The crystal, X1, may be replaced with an external clock source.

4.3 CMX994 Interface

When operating the 7131/7141FI-3.x in I/Q mode the interface to the CMX994 Direct Conversion Receiver shown in Figure 6 should be used. Component values are shown in Table 2, where values are not shown refer to the CMX994 datasheet.

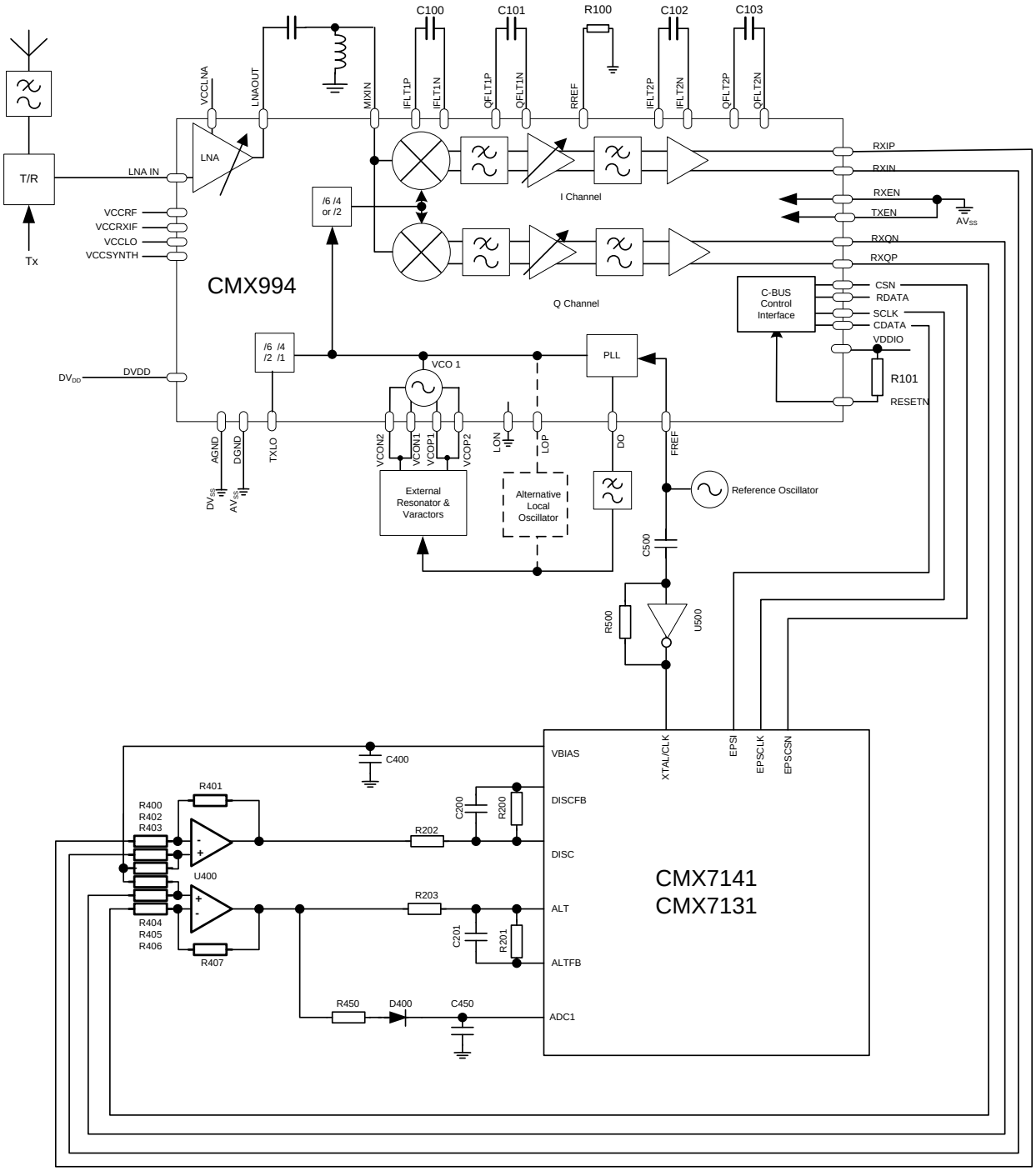


Figure 6 CMX994 Interface

Table 2 Recommended External Components when using CMX994

R100	10kΩ	C100	1.5nF	C500	1nF
R101	100kΩ	C101	1.5nF	R500	100kΩ
		C102	3.9nF	D400	MMBD1503A
R200	100kΩ	C103	3.9nF	U500	e.g. SN74AHC1G04DRL
R201	100kΩ				
R202	100kΩ	C201	100pF		
R203	100kΩ	C202	100pF		
		C450	3.3pF	U400	e.g. LM6132
R450	22kΩ	C400	100nF	R400-407	10kΩ

5 General Description

5.1 Features

7131/7141FI-3.x for the CMX7131/CMX7141 is intended for use in half duplex digital PMR equipment using 4-FSK modulation at 4800 bps suitable for 6.25kHz channel systems, or 9600 bps for 12.5kHz systems.

Much of the NXDN standard air interface protocol is embedded within the CMX7131/CMX7141 operation namely:

Air Interface Physical Layer 1

- 4-FSK modulation and demodulation (4.8 and 9.6 kbps)
- Bit and symbol definition
- Frequency and symbol synchronisation
- Transmission burst building and splitting

Air Interface – Data Link Layer 2

- Channel coding (FEC, CRC)
- Interleaving, de-interleaving and bit ordering
- Frame building and synchronising (Conventional and Class-D Trunking)
- Burst and parameter definition
- Interfacing of voice applications (voice data) with the Physical Layer
- Data bearer services
- Exchanging signalling and/or user data with the Call Control Layer
- Automatic RAN detection

The 7131/7141FI-3.x has two receiver interface modes: Limiter/Discriminator (LD) mode is selected by default and is compatible with 7131/7141FI-3.0.x for conventional limiter/discriminator receivers; I/Q mode is tailored for operation with the CMX994 Direct Conversion Receiver IC. The transmitter can provide a conventional output suitable for 2-point modulation or for an I/Q interface.

A flexible power control facility allows the device to be placed in its optimum powersave mode when not actively processing signals.

The device includes a crystal clock generator, with buffered output, to provide a common system clock if required.

A block diagram of the device is shown in Figure 1.

The signal processing blocks can be routed from any of the three DISC/ALT/MIC input pins.

Other Functions Include:

- Automatic Tx sequencer simplifies host control
- RAMDAC operation
- TxENA and RxENA hardware signals
- Two-point or I/Q modulation outputs
- Hard or Soft data options

Auxiliary Functions:

- Two programmable system clock outputs

- Two auxiliary ADCs with four selectable external input paths
- Four auxiliary DACs, one with built-in programmable RAMDAC
- Two RF PLLs (CMX7131 only)

Interface:

- Optimised C-BUS (4 wire high speed synchronous serial command/data bus) interface to host for control and data transfer
- Open drain IRQ to host
- SPI bus interface for speech codec to support the AMBE+2 vocoder
- Two GPIO pins
- Serial Memory boot mode (L/D mode only)
- C-BUS (host) boot mode
- Auxiliary C-BUS interface to CMX994 Direct Conversion Receiver

5.2 System Design

System architecture supports an external vocoder, implementing the AMBE+2 algorithm, such as the AMBE-3000^{TM} or as part of the host uC implementation using SPI-Codec mode, in which the CMX7131/CMX7141 acts as an external audio codec attached to the vocoder. The host must issue all control commands to the vocoder and also transfer coded data packets between the vocoder and CMX7131/CMX7141. The device will automatically enable/disable the activity on the SPI-Codec port when a voice call is in progress.

In SPI-Codec mode, signed 16-bit linear PCM audio samples are transferred at 8ksps. When this mode is selected:

In Tx: the CMX7131/CMX7141 microphone input should be routed from MIC to Input2. This signal is lowpass filtered, converted to PCM data and then output on the EPSI pin of the SPI-Codec port for the external vocoder to process.

In Rx: the CMX7131/CMX7141 AUDIO output should be routed from Output1. PCM data samples are read from the EPSO pin of the SPI-Codec port, then filtered and output via the audio output attenuator.

VOC_DIS	SPI-Codec	Port Mode	Activity
0	1	SPI	SPI Port enabled during Rx or Tx, PCM data from MIC/to AUDIO passed over SPI bus

The automatic enable/disable of the SPI-Codec port during Rx and Tx may be overridden by setting the VOC_DIS bit in the Modem Configuration register, $C7:b7. In this situation, the activity on the SPI-Codec port is determined by the host setting/clearing the SPI-Codec ENA, $B1:b0.

VOC_DIS	SPI-Codec	Port Mode	Activity
1	0	SPI	SPI Port disabled
1	1	SPI	SPI Port enabled, PCM data from MIC/to AUDIO passed over SPI bus

5.2.1 I/Q and Full-rate Limitations

Due to the increased signal processing load required to support I/Q and full-rate modes, this combination of functionality is only available when this Function Image is hosted on CMX7241/CMX7341 hardware:

Table 3 I/Q and Full Rate compatibility

Mode	Rate	CMX7131/CMX7141	CMX7241/CMX7341
Limiter Discriminator	Half Rate	OK	OK
	Full Rate	OK	OK
I/Q	Half Rate	OK	OK
	Full Rate	Not Allowed	OK

5.2.2 Vocoder Implementation

All payload data (including voice traffic channel data) is routed through the main C-BUS to the host. The host can then transfer it to/from the vocoder over a suitable port supported by the chosen vocoder. Typically vocoders do not include audio Digital-to-Analogue and Analogue-to-Digital converters, so the CMX7131/CMX7141 can be configured to use its auxiliary C-BUS as an SPI interface and use its built-in DAC/ADC's as audio converters as shown in Figure 7.

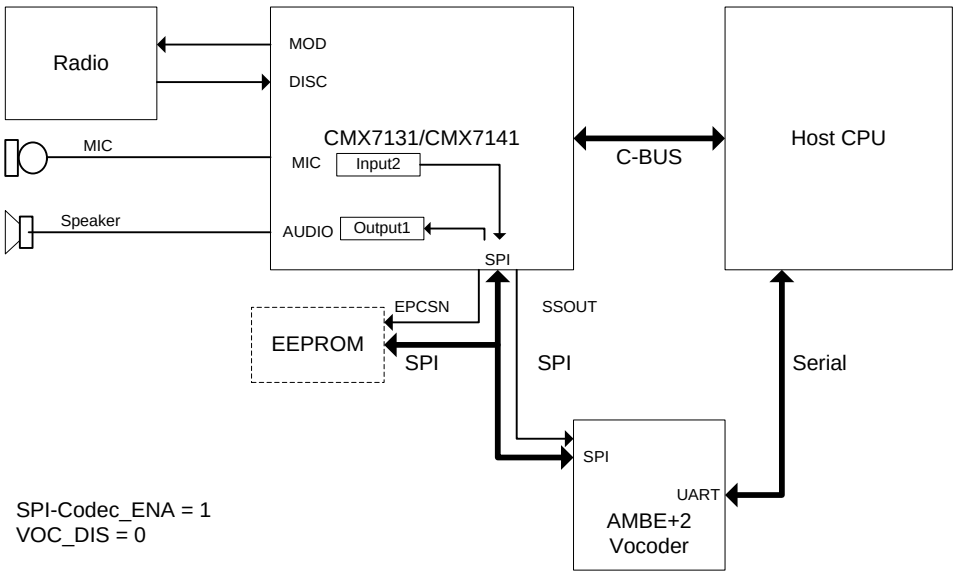
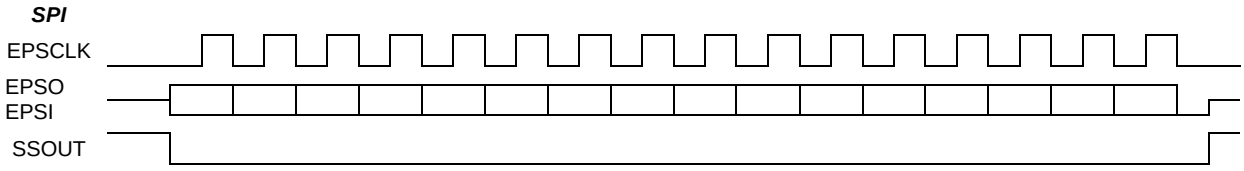


Figure 7 NXDN Vocoder Connection

Table 4 SPI-Codec Format



Note: There are 16 SCLK pulses per data transfer. The default SCLK rate is 2MHz.

5.2.3 Data Transfer

When transmitting, an initial block of payload or control channel data will need to be loaded from the host into the C-BUS TxData registers. The CMX7131/CMX7141 can then format and transmit that data while at the same time loading in the following data blocks from the host or vocoder.

When receiving, the host needs to consider that when a signal is received over the air there will be a processing delay while the CMX7131/CMX7141 filters, demodulates and decodes the output data before

presenting it to the host. For best performance voice payload data can be output in soft-decision (4-bit log-likelihood ratio) format although this mode increases the data transfer rate over C-BUS by a factor of four.

5.2.4 Serial Memory Connection (LD Mode only)

In all cases, the auxiliary C-BUS/SPI-Codec bus is shared with the serial memory bus which may be used to load the contents of the Function Image. Bus conflicts are avoided by the use of an additional Chip Select signal (SSOUT). If this feature is not used then the EPSCSN pin should be left un-connected. Serial Memory may not be used in I/Q interface mode.

5.2.5 CMX994 Connection (I/Q Mode only)

The CMX994 can be connected via the C-BUS connection in place of the serial memory (Table 5). This allows the CMX994 to be used along with the AMBE-3000^{TM} Vocoder.

Note that the data and clock connections to the CMX994 are common with the Vocoder, so the data traffic on the interface is a potential source of noise/interference in the radio.

Table 5 CMX994 Connections

CMX7131/CMX7141 Pin:	CMX994 Pin:
EPSCSN	CSN
EPSI	CDATA
EPSCLK	SCLK
No connection	RDATA

The operation of the CMX994 is generally automatic, however specific data may be written to CMX994 registers using the pass-through mode available using register $C8. For example if the CMX994 PLL and VCO are used in the radio design then it is necessary to programme the appropriate frequency data to the CMX994 PLL-M Divider, PLL N-Divider and VCO Control registers using the pass-through mode before attempting reception.

5.2.6 Hardware AGC – AuxADC1 Connection

In I/Q mode, the AuxADC1 input can be used to improve the adjacent/alternate channel rejection with the addition of suitable external components, see Figure 6. This function provides a broadband signal detector which is used in the AGC process. This is required to prevent the DISC/ALT ADC inputs limiting internally in the presence of alternate channel signals, which are attenuated by the inherent filtering of the ADC.

This functionality is enabled by setting:

- Program Block P2.0:b8=1 (enable hardware AGC)
- Program Block P3.0 = $F002 (AuxADC1 averaging = 2)
- $CD = $4205 (hi threshold)
- $CD = $0200 (lo threshold)
- $A7 = $0030 (turn AuxADC1 on)

Note that threshold levels may need adjustment to suit particular hardware implementations

.

5.2.7 RSSI Measurement (LD Mode only)

The AuxADC provided by the CMX7131/CMX7141 can be used to detect the squelch or RSSI signal from the RF section while the device is in Rx or Idle mode. This allows a significant degree of powersaving within the CMX7131/CMX7141 and avoids the need to wake the host up unnecessarily. The host programmable AuxADC thresholds allow for user selection of squelch threshold settings.

5.2.8 RSSI Measurement (I/Q Mode only)

In I/Q mode the RSSI is calculated from the signal levels present at the I and Q inputs and the AGC levels currently in use. Figure 8 shows a typical response.

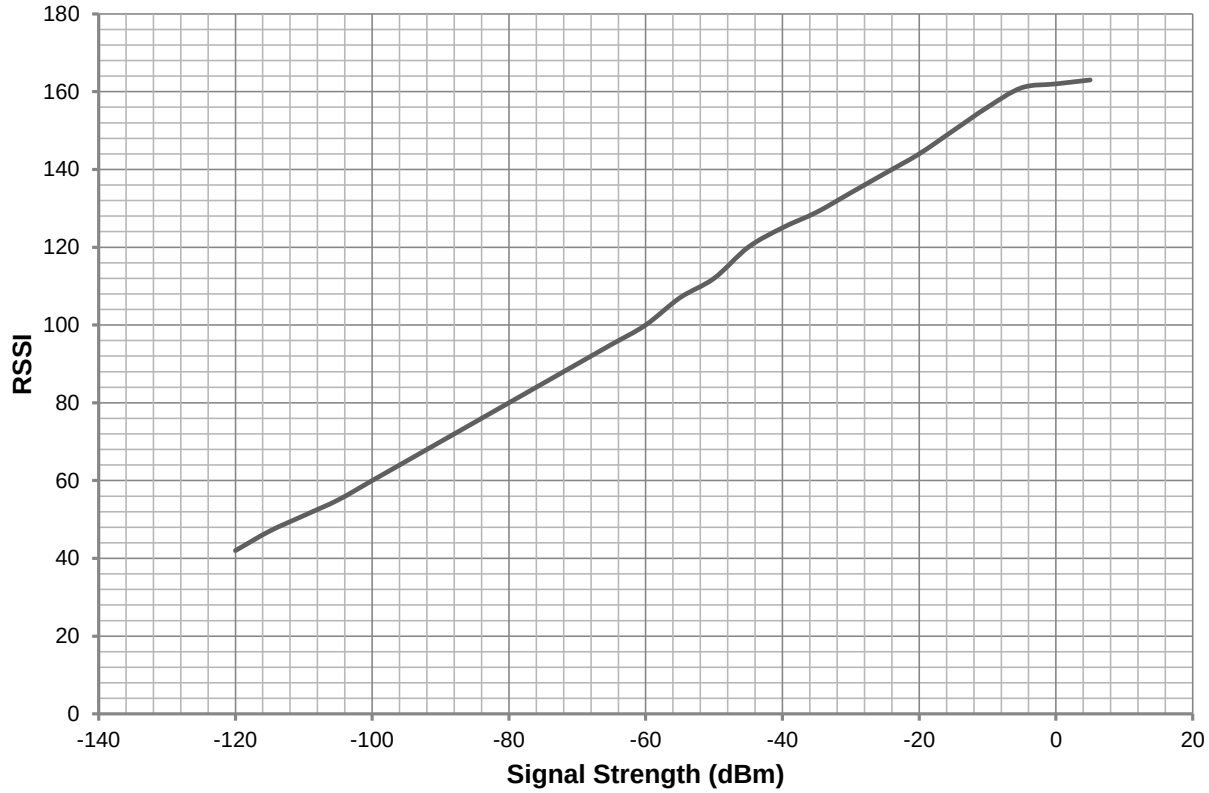


Figure 8 RSSI in I/Q Mode

5.3 Introduction

This modem runs at 4800 / 9600 bps, suitable for a 6.25 / 12.5kHz bandwidth RF channel. It has been designed such that, when combined with suitable RF, host controller, vocoder and appropriate control software, it meets the requirements of the NXDN™ 4-FSK standard.

The NXDN standard specifies the AMBE+2 Voice Coding algorithm which is supported by transferring all payload data through the host using the main C-BUS interface.

The standard requires a 4-FSK modulation scheme with an over-air bit rate of 4800 / 9600 bps (2400 / 4800 symbols per second). FI-3.x supports:

- 4800 bps (half rate) Conventional mode using RDCH channel formatting.
- 4800 bps (half rate) Class-D Trunking using RTCH2 channel formatting
- 9600 bps (full rate) Conventional mode using RDCH channel formatting.

5.3.1 Modulation

The NXDN 4-FSK modulation scheme operates in a 6.25 / 12.5kHz channel bandwidth with an over-air bit rate of 4800 / 9600 bps (2400 / 4800 symbols per second). RRC filters are implemented at both Tx and Rx with a filter “alpha” of 0.2. The maximum frequency error is +/- 625Hz and the CMX7131/CMX7141 can adapt to the maximum time base clock drift of 2ppm over the duration of a 180-second burst. Figure 11 shows the basic parameters of the 4FSK modulation, symbol mapping and filtering requirements.

Figure 9 and Figure 10 show a transmitted PRBS waveform, as recorded on a spectrum analyser in 36k span and zero-span mode, having been 2-point modulated using a suitable RF transmitter in half-rate mode..

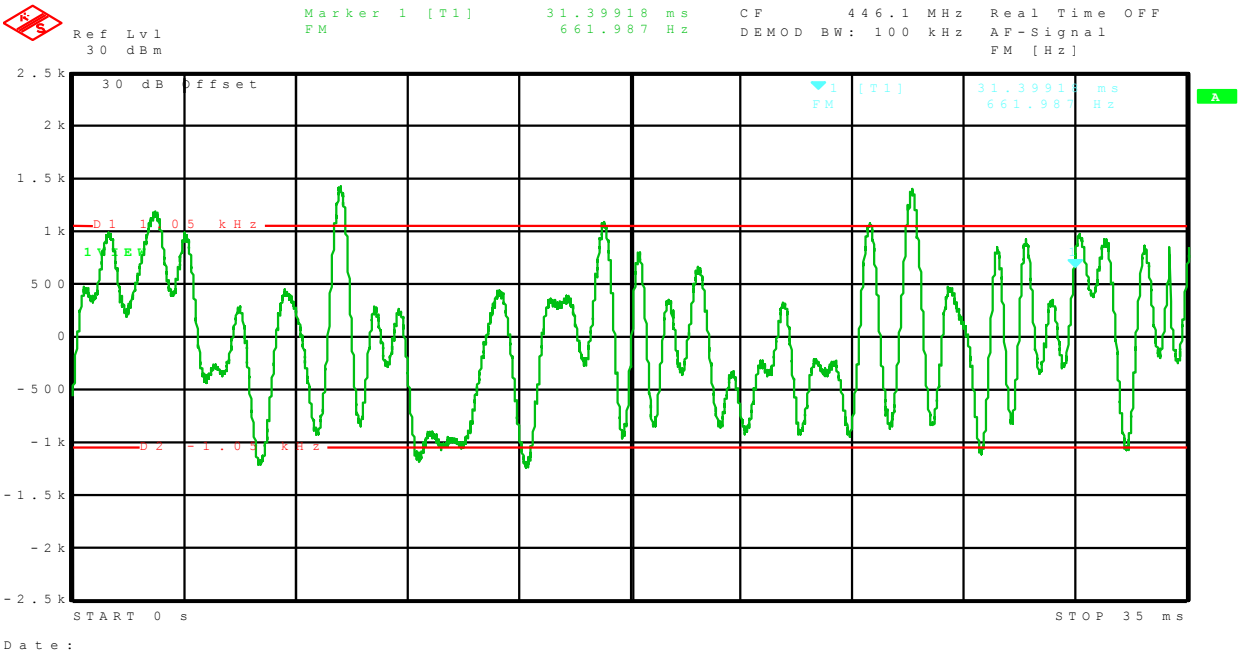


Figure 9 4800 bps 4-FSK PRBS Waveform – Modulation

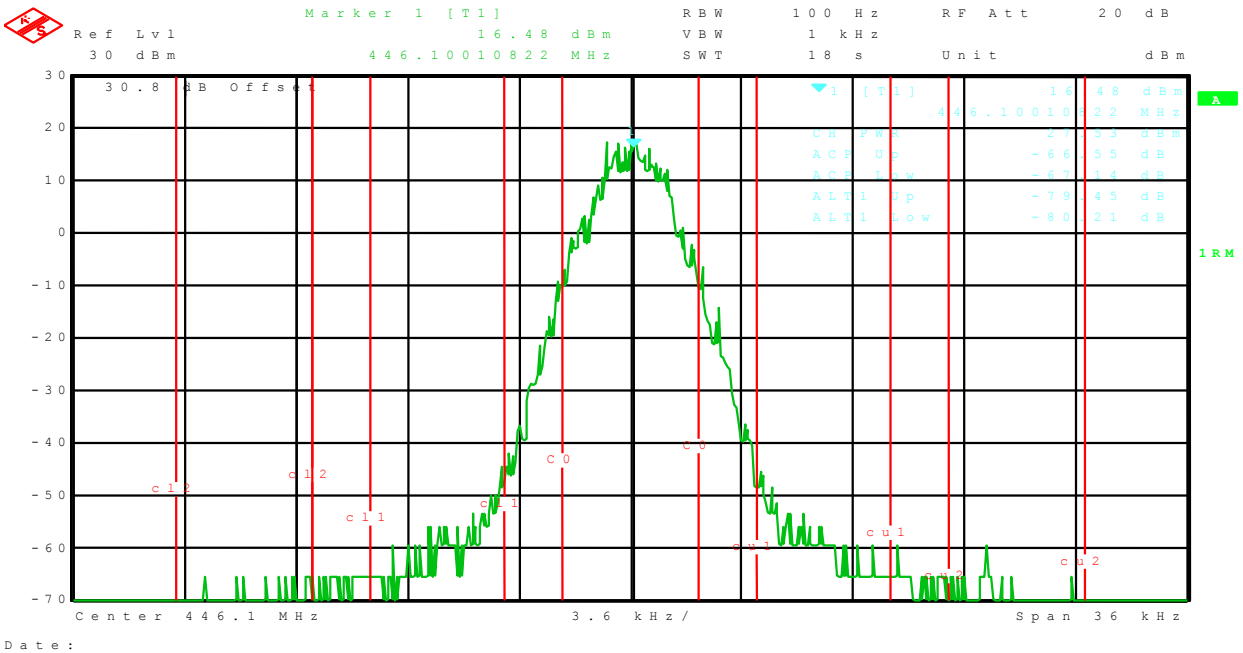
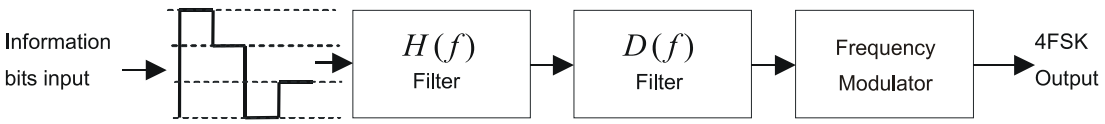


Figure 10 4800 bps 4-FSK PRBS Waveform – Spectrum

Tx Baseband Filter



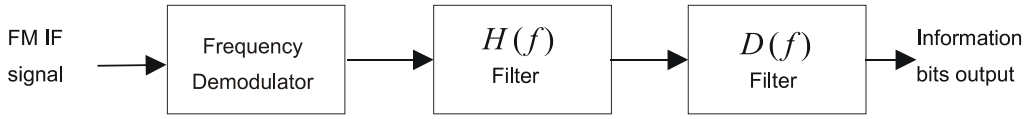
$$|H(f)| = \begin{cases} 1 & , \quad 0 \le |f| < (1-\alpha)/2T \\ \cos\left[(T/4\alpha)(2\pi|f| - \pi(1-\alpha)/T)\right] & , \quad (1-\alpha)/2T \le |f| < (1+\alpha)/2T \\ 0 & , \quad (1+\alpha)/2T \le |f| \end{cases}$$

$$\alpha = 0.2 \qquad T = 1/2400$$

$$|D(f)| = \frac{\sin(\pi fT)}{\pi fT}$$

Di-bit	Symbol
01_2	+3
00_2	+1
10_2	-1
11_2	-3

Rx Baseband Filter



$$|H(f)| = \begin{cases} 1 & , \quad 0 \le |f| < (1-\alpha)/2T \\ \cos\left[(T/4\alpha)(2\pi|f| - \pi(1-\alpha)/T)\right] & , \quad (1-\alpha)/2T \le |f| < (1+\alpha)/2T \\ 0 & , \quad (1+\alpha)/2T \le |f| \end{cases}$$

$$\alpha = 0.2 \qquad T = 1/2400$$

$$|D(f)| = \frac{\pi fT}{\sin(\pi fT)}$$

Figure 11 Modulation Characteristics

Note: for 4800 bps T=1/2400, for 9600 bps T=1/4800

Table 6 Modulation Deviation

Di bit	Symbol	Deviation	
		4800 bps	9600 bps
01	+3	+1050 Hz	+2400 Hz
00	+1	+350 Hz	+800 Hz
10	-1	-350 Hz	-800 Hz
00	-3	-1050 Hz	-2400 Hz

5.3.2 Internal Processing

The CMX7131/CMX7141 operates as a half-duplex device, either receiving signals from the RF circuits in Rx mode, or sourcing signals to the RF circuits in Tx mode. It also has a low power IDLE mode to support battery saving protocols. The internal data processing blocks for Tx and Rx modes are illustrated in Figure 12. Additional processing in I/Q Mode is shown in Figure 13.

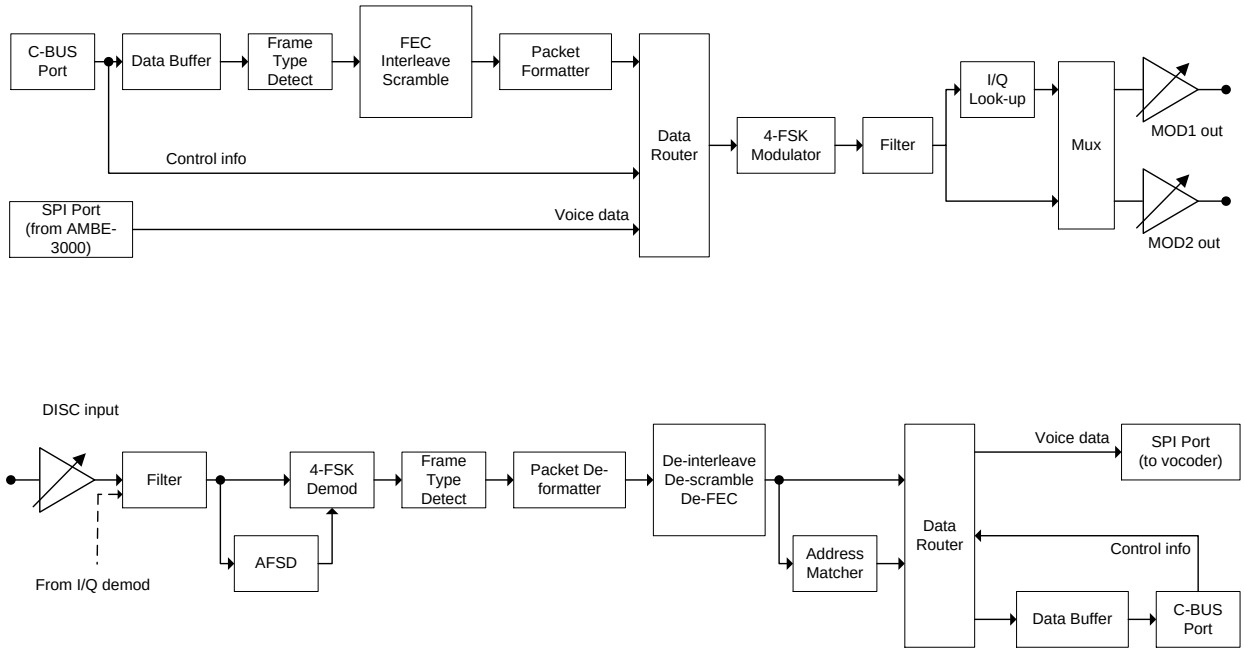


Figure 12 Internal Data Blocks (LD Mode)

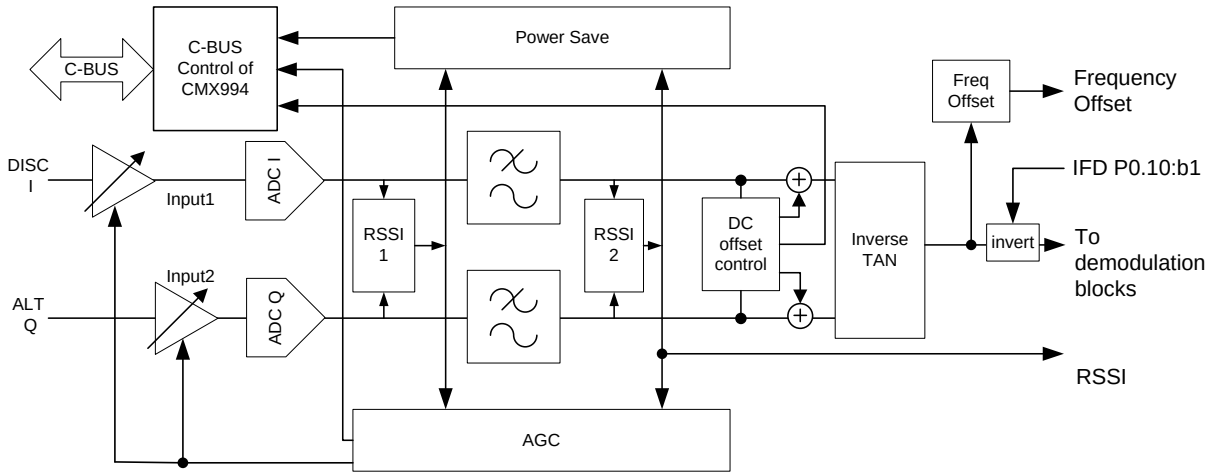


Figure 13 Additional Internal Data Processing in I/Q Mode

5.3.3 Frame Sync Detection and Demodulation

The analogue signal from the receiver may be from either a CMX994 I/Q interface or a limiter/discriminator (LD) output. The signal(s) from the RF section should be applied to the CMX7131/CMX7141 input(s) (normally the DISC input for LD Rx and DISC and ALT inputs for I/Q Rx). The signals can be adjusted to the correct level either by selection of the feedback resistor(s) or using the

CMX7131/CMX7141 Input Gain settings. In LD mode the signal is filtered using a Root-Raised Cosine filter and Inverse Rx Sinc filter matching the filters applied in the transmitter, then passed to the AFSD (Automated Frame Sync Detector) block which extracts symbol and frame synchronisation. During this process the 4FSK demodulator and the data-processing sections that follow are dormant to minimise power consumption. When frame synchronisation has been achieved the AFSD section is powered down, and timing and symbol-level information is passed to the 4FSK demodulator which starts decoding the subsequent data bits. The CMX7131/CMX7141 can detect the end of a burst by scanning the received control channel fields and will automatically disable the demodulator and restart frame sync search when required without host intervention.

In I/Q mode, filtering is applied to the input signals and dc offsets are removed before an inverse tangent function performs the FM demodulation function. The output of this stage has an offset depending on the frequency error of the received signal compared to the nominal frequency of the receiver. This offset is removed after which the signal chain is then the same as the LD case. In I/Q mode the CMX7131/CMX7141 provides measurements of frequency error and RSSI (which are not available in LD mode).

An NXDN™ call consists of a series of 80ms frames, each starting with a 20-bit Synchronisation Word (SW). The first frame is preceded by a Preamble sequence, and the CMX7131/CMX7141 uses the last 18 bits of the Preamble together with the first Synchronisation Word to detect the start of a transmission. This is reported to the host by setting the FS1 Detect bit in the Status register.

Last 9 Symbols of Preamble: `xx11 0111 0101 1111 1101 ($375FD)`

Synchronisation Word: `1100 1101 1111 0101 1001 ($CDF59)`

The CMX7131/CMX7141 can optionally also detect the Synchronisation Word sequence in isolation to perform “late entry” into an existing call. This is reported to the host by setting the FS2 Detect bit in the Status register. The short length of the Synchronisation Word gives a high probability of false detections, so by default the CMX7131/CMX7141 will only generate an initial FS2 Detect if two successive Synchronisation Words are detected at the correct frame spacing in the received signal.

Additionally, once initial synchronisation has been achieved with an FS1 or FS2 Detect, it can later be re-established from a single Synchronisation Word received within ±2 symbols of the original frame timing. This mode slightly increases power consumption in order to maintain the symbol timer through Rx-Tx-Rx or Rx-IDLE-Rx transitions and hence is selectable using b13 of the modem configuration register, $C7. Note that this also requires b8 of $C7 to be set in order to enable FS2 detects.

When frame synchronisation has been achieved and the 4FSK demodulator has been enabled, Frame Sync detection is switched off and any subsequent Preamble or Synchronisation Word sequences in the received data are not reported to the host.

Table 7 NXDN Half Rate Frame Format – Audio Communication

bits:	>24	20	16	60				144								144							
	P	SW	LI	SACCH				FACCH1								FACCH1							
		SW	LI	SACCH				TCH1				TCH2				TCH3				TCH4			
		SW	LI	SACCH				TCH1				TCH2				TCH3				TCH4			
		SW	LI	SACCH				TCH1				TCH2				TCH3				TCH4			
		SW	LI	SACCH				TCH1				TCH2				TCH3				TCH4			
	Repeat until PTT released….																						
		SW	LI	SACCH				FACCH1								FACCH1							

Table 8 NXDN Frame Format – Data Communication

bits:	>24	20	16	348
	P	SW	LI	UDCH1 or FACCH2

Table 9 NXDN Full Rate Frame Format – Audio Communication

bits:	>24	20	16	60	144		144	
	P	SW	LI	SACCH	FACCH1		FACCH1	
		SW	LI	SACCH	TCH1	TCH2	TCH3	TCH4
		SW	LI	SACCH	FACCH1	FACCH1	FACCH1	FACCH1
		SW	LI	SACCH	TCH1	TCH2	TCH3	TCH4
		SW	LI	SACCH	FACCH1	FACCH1	FACCH1	FACCH1
		SW	LI	SACCH	TCH1	TCH2	TCH3	TCH4
		SW	LI	SACCH	FACCH1	FACCH1	FACCH1	FACCH1
		SW	LI	SACCH	TCH1	TCH2	TCH3	TCH4
		SW	LI	SACCH	FACCH1	FACCH1	FACCH1	FACCH1
	Repeat until PTT released….							
		SW	LI	SACCH	FACCH1		FACCH1	

- P = Preamble (optional)
- SW = Synchronisation Word
- FS1 = 18 bits Preamble + 20 bits SW
- FS2 = 20 bits SW
- LI = LICH (Link Information Channel)
- SACCH = Slow Associated Control Channel
- FACCH1 = Fast Associated Control Channel 1 (144 bits)
- FACCH2 = Fast Associated Control Channel 2 (348bits)
- TCHx = Traffic/Payload Data (72 bits)
- UDCH1 = User Data Channel 1 (348 bits)
- In Tx and Rx mode, the Preamble and Synchronisation Word are handled automatically and do not need to be loaded by the host.
- It is possible to substitute FACCH1 blocks for TCH blocks during a call (frame stealing), in which case the vocoder should either be fed a silence frame or repeat its last data.
- Note that the CAC format is not supported.
- For Class-D operation, additional formats are supported by setting $C7:b6:
- FACCH1+G = Fast Associated Control Channel 1 (144 bits) + Guard Time (144 bits of no signal)
- FACCH3 = Fast Associated Control Channel 3 (288 bits)
- UDCH2 = User Data Channel 2 (288 bits)

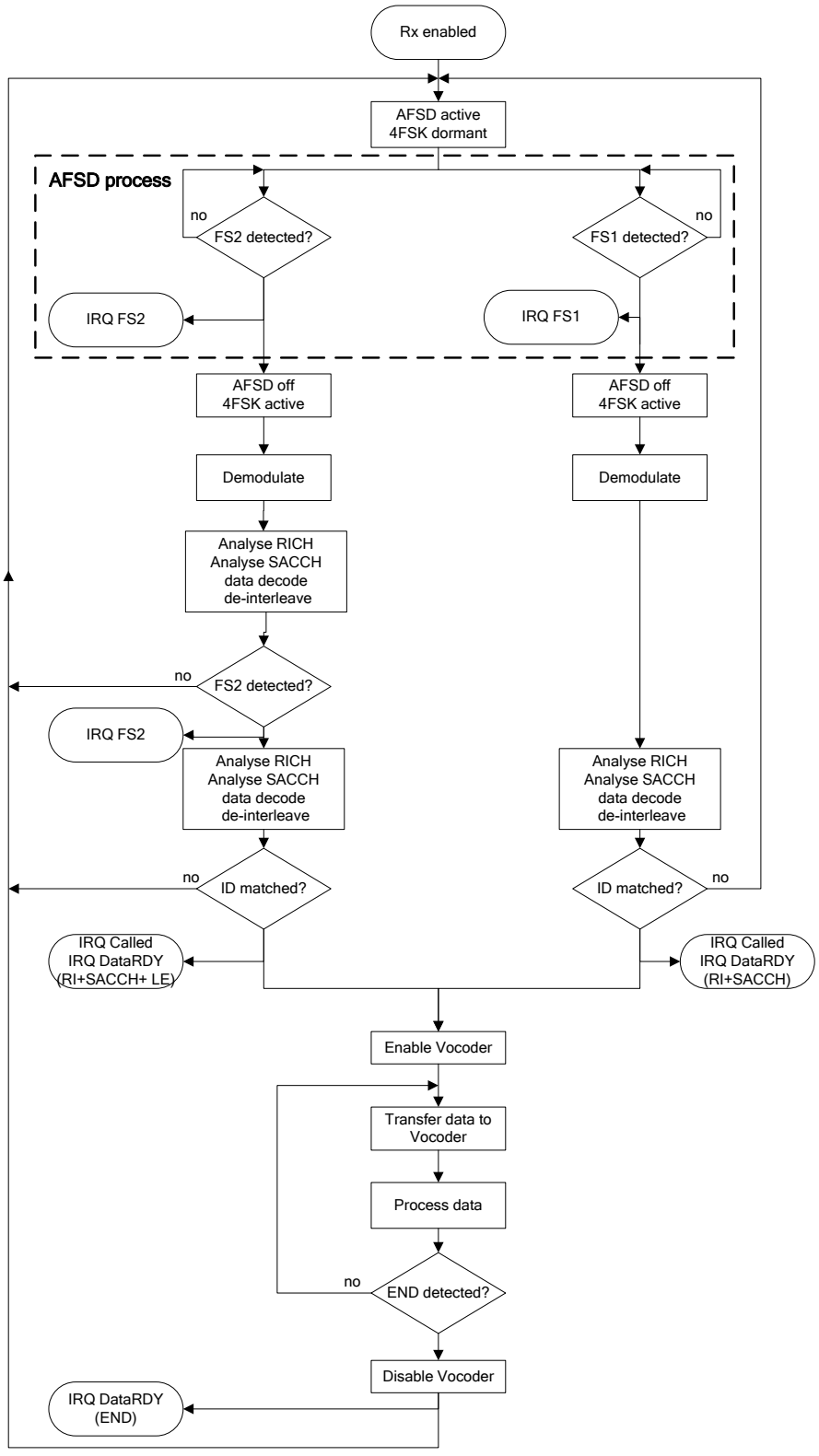


Figure 14 FS Detection

5.3.4 FEC and Coding

The CMX7131/CMX7141 implements all CRCs, convolutional codes, interleaving and scrambling required by the NXDN standard for 4800bps Conventional Mode operation. CRC failures in control channel fields and coded data blocks are indicated to the host by issuing an "Event" IRQ with a corresponding error code in the Modem Status register, $C9. This relieves the host of a substantial processing load and has the added advantage of reducing the complexity and timing constraints of interfacing between the host, vocoder and CMX7131/CMX7141.

Table 10 Frame Types

Frame type	Un-coded data bits (C-BUS interface)	Coded data bits (over-air)	Notes:
LICH	7	16	
SACCH	8 + 18	60	Radio Access Number in the SU field
FACCH1	80	144	
FACCH2	8 + 176	348	Radio Access Number in the SU field
UDCH1	8 + 176	348	Radio Access Number in the SU field
TCHx	72	72	Coding applied by vocoder
FACCH3	160	288	Class-D only
UDCH2	160	288	Class-D only

Note: If the "Soft data" function is enabled, in Rx mode ($C7:b4), TCHx data will be reported as a 4-bit LLR code per data bit (suitable for decoding by the AMBE+2 vocoder).

5.3.5 Voice Coding

The CMX7131/CMX7141 supports an external vocoder by routing voice payload data over the main C-BUS interface and through the host. In this mode, all vocoder control and data transfers must be managed by the host.

Voice data transferred to the external vocoder in Rx mode may use soft decision (4-bit log-likelihood ratio) format, although it increases the required data transfer rate over C-BUS by a factor of four.

5.3.6 Radio Performance Requirements

In LD mode, for optimum performance, the signal should not be significantly degraded by filters that are excessively narrow and/or cause significant group delay distortion. Care should be taken when interfacing the device to the radio circuits to maintain the frequency and phase response (both low and high end), in order to achieve optimum performance. Test modes are provided to assist in both the initial design and production set-up procedures.

In I/Q mode the recommended interfacing to the CMX994 should be used; see section 4.3. The CMX7131/CMX7141 includes digital filters to provide adjacent channel rejection while compensating for the in-band response of the CMX994 I/Q filters.

Further information and application notes can be found at http://www.cmlmicro.com.

6 Detailed Descriptions

6.1 Xtal Frequency

The CMX7131/CMX7141 is designed to work with an external frequency source of 19.2MHz. If this default configuration is not used then Program Register Block 3 must be loaded with the correct values to ensure that the device will work to specification with the user selected clock frequency. A table of common values can be found in Table 11. Note the maximum Xtal frequency is 12.288MHz although an external clock source of up to 24MHz can be used.

The register values in Table 1 are shown in hex, the default settings are shown in bold, and the settings which do not give an exact setting (but are within acceptable limits) are in italics. The new P3.2-3 settings take effect following the write to P3.3. (The settings in P3.4-7 are implemented on a change to Rx or Tx mode.)

Table 11 Xtal/Clock Frequency Settings for Program Block 3

Program Register			External Frequency Source (MHz)							
			3.579	6.144	9.216	12.0	12.8	16.368	16.8	**19.2**
P3.2	Idle	GP Timer	*$017*	$018	$018	$019	$019	*$018*	$019	**$018**
P3.3		VCO output and AUX clk divide	*$085*	$088	$08C	*$10F*	*$110*	*$095*	*$115*	**$099**
P3.4	Rx or Tx	Ref clk divide	*$043*	$040	$060	$07D	$0C8	$155	$15E	**$0C8**
P3.5		PLL clk divide	*$398*	$200	$200	$200	$300	$400	$400	**$200**
P3.6		VCO output and AUX clk divide	*$140*	$140	$140	$140	$140	$140	$140	**$140**
P3.7		Internal ADC / DAC clk divide	*$008*	$008	$008	$008	$008	$008	$008	**$008**

6.2 Host Interface

A serial data interface (C-BUS) is used for command, status and data transfers between the CMX7131/CMX7141 and the host µC; this interface is compatible with microwire and SPI. Interrupt signals notify the host µC when a change in status has occurred and the µC should read the status register across the C-BUS and respond accordingly. Interrupts only occur if the appropriate mask bit has been set. See section 6.5.2.

The CMX7131/CMX7141 will monitor the state of the C-BUS registers that the host has written to every 250µs (the C-BUS latency period) hence it is not advisable for the host to make successive writes to the same C-BUS register within this period.

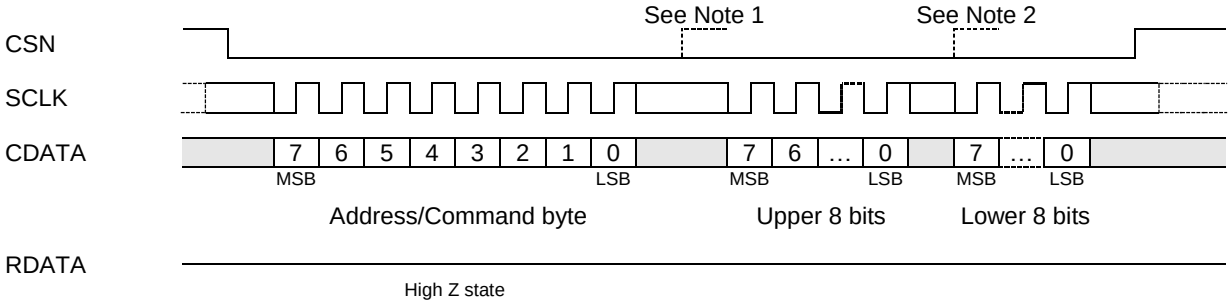
6.2.1 C-BUS Operation

This block provides for the transfer of data and control or status information between the CMX7131/CMX7141's internal registers and the host µC over the C-BUS serial interface. Each transaction consists of a single address byte sent from the µC which may be followed by one or more data byte(s) sent from the µC to be written into one of the CMX7131/CMX7141's Write Only Registers, or one or more data byte(s) read out from one of the CMX7131/CMX7141's Read Only Registers, as shown in Figure 15.

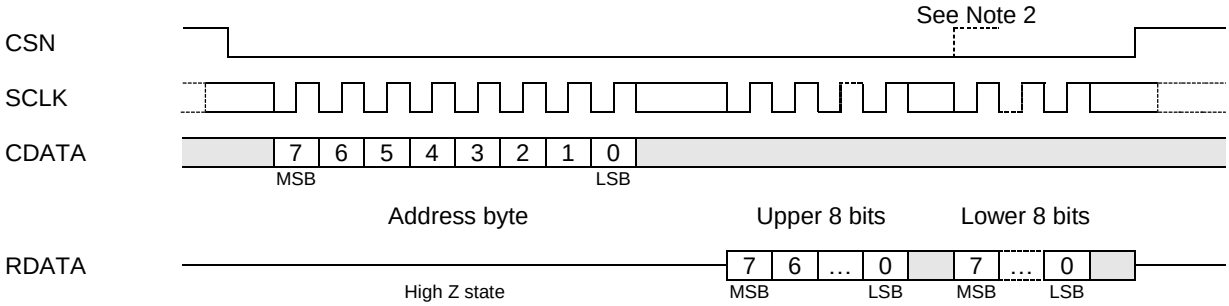
Data sent from the µC on the CDATA (Command Data) line is clocked into the CMX7131/CMX7141 on the rising edge of the SCLK (Serial Clock) input. RDATA (Reply Data) sent from the CMX7131/CMX7141 to the µC is valid when SCLK is high. The CSN line must be held low during a data transfer and kept high between transfers. The C-BUS interface is compatible with most common µC serial interfaces and may also be easily implemented with general purpose µC I/O pins controlled by a simple software routine.

The number of data bytes following an address byte is dependent on the value of the address byte. The most significant bit of the address or data are sent first. For detailed timings see section 7.2. Note that, due to internal timing constraints, there may be a delay of up to 250µs between the end of a C-BUS write operation and the device reading the data from its internal register.

C-BUS Write:



C-BUS Read:



Data value unimportant

Repeated cycles

Either logic level valid (and may change)

Either logic level valid (but must not change from low to high)

Figure 15 C-BUS Transactions

Notes:

1. For Command byte transfers only the first 8 bits are transferred ($01 = Reset).
2. For single byte data transfers only the first 8 bits of the data are transferred.
3. The CDATA and RDATA lines are never active at the same time. The Address byte determines the data direction for each C-BUS transfer.
4. The SCLK input can be high or low at the start and end of each C-BUS transaction.
5. The gaps shown between each byte on the CDATA and RDATA lines in the above diagram are optional, the host may insert gaps or concatenate the data as required.

6.3 Function Image™ Loading

***NOTE**:FI loading from serial memory is not supported when FI-3.x is used in I/Q mode because the serial memory interface is used for CMX994 control.*

The Function Image™ (FI), which defines the operational capabilities of the device, is obtained from the CML Technical Portal, following registration. This is in the form of a 'C' header file which can be included into the host controller software or programmed into an external serial memory. The maximum possible size of a Function Image™ is 46kbytes, although a typical FI will be less than this. Note that the BOOTEN pins are only read at power-on or following a C-BUS General Reset and must remain stable throughout the FI loading process. If the CMX994 is to be used, then the BOOTEN pins MUST both be held high once the FI load has completed, otherwise they are ignored by the CMX7131/CMX7141 until the next power-up or C-BUS General Reset.

The BOOTEN pins are both fitted with internal low current pull down devices.

For C-BUS load operation, both pins should be pulled high by connecting them to DV_{DD} either directly or via a 220kΩ resistor (see Table 12).

For serial memory load, only BOOTEN1 needs to be pulled high in a similar manner, however, if it is required to program the serial memory in-situ from the host, either a jumper to DV_{DD} or a link to a host I/O pin should be provided to pull BOOTEN2 high when required (see Table 12). The serial memory interface is shared with the Auxiliary C-BUS port which controls the CMX6x8 Vocoder using a separate chip select (SSOUT) pin. During boot operations, the SSOUT will be disabled. Once the boot operation has completed, the serial memory chip select (EPSCSN) will be disabled and the SSOUT will become operational.

Once the FI has been loaded, the CMX7131/CMX7141 performs these actions:

(1) the product identification code ($7141 or $7131) is reported in C-BUS register $C5
(2) the FI version code is reported in C-BUS register $C9
(3) the two 32-bit FI checksums are reported in C-BUS register pairs $A9, $AA and $B8, $B9
(4) the device waits for the host to load the 32-bit Device Activation Code to C-BUS register $C8
(5) once activated, the device initialises fully, enters IDLE mode and becomes ready for use, and the Programming Flag (bit 0 of the Status register) will be set.

The checksums should be verified against the published values to ensure that the FI has loaded correctly. Once the FI has been activated, the checksum, product identification and version code registers are cleared and these values are no longer available. If an invalid activation code is loaded, the device will report the value $DEAD in register $A9 and must be power cycled before an attempt is made to re-load the FI and re-activate.

Both the Device Activation Code and the checksum values are available from the CML Technical Portal.

Table 12 BOOTEN Pin States

	BOOTEN2	BOOTEN1
C-BUS Host load	1	1
reserved	1	0
Serial Memory load	0	1
No FI load	0	0

Note: Following a General reset, reloading of the Function Image is strongly recommended.
Note: For operation with the CMX994, BOOTEN1 and BOOTEN2 MUST be held high at all times.

6.3.1 FI Loading from Host Controller

The FI can be included into the host controller software build and downloaded into the CMX7131/CMX7141 at power-up over the C-BUS interface. The BOOTEN pins must be set to the C-BUS load configuration, the CMX7131/CMX7141 powered up and placed into Program Mode, the data can then be sent directly over the C-BUS to the CMX7131/CMX7141.

If the host detects a brownout, the BOOTEN state should be set to re-load the FI. A General Reset should then be issued and the appropriate FI load procedure followed.

Each time the Programming register, $C8, is written, it is necessary to wait for the PRG flag (Status register ($C6) b0) to go high before another write to $C8. The PRG flag going high confirms the write to the Programming register has been accepted. The PRG flag state can be determined by polling the Status register or by unmasking the interrupt (Interrupt Mask register, $CE, b0).

The download time is limited by the clock frequency of the C-BUS, with a 5MHz SCLK, it should take less than 500ms to complete (host dependent).

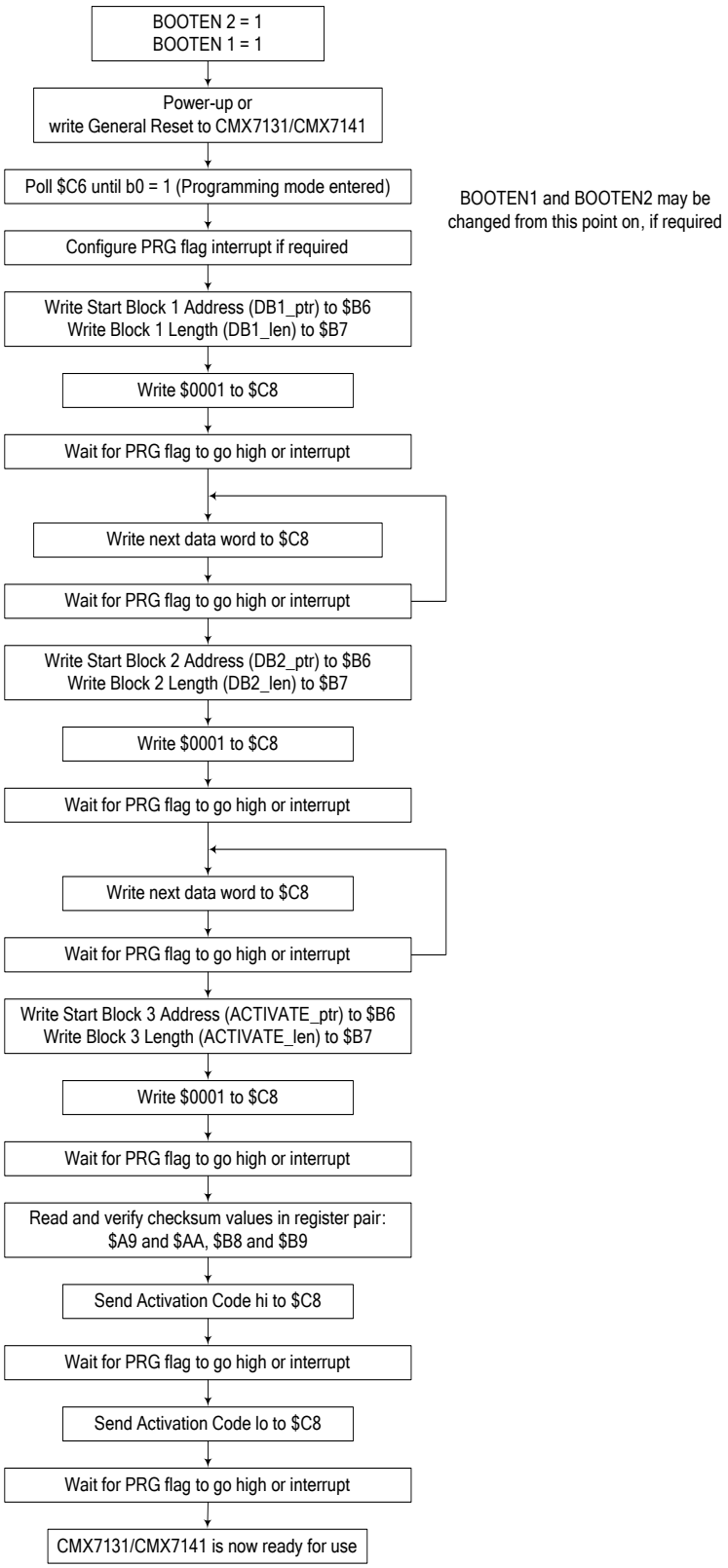


Figure 16 FI Loading from Host

6.3.2 FI Loading from Serial Memory

The FI must be converted into a format for the serial memory programmer (normally Intel Hex) and loaded into the serial memory either by the host or an external programmer. The CMX7131/CMX7141 needs to have the BOOTEN pins set to serial memory load, and then, on power-on, or following a C-BUS General Reset, the CMX7131/CMX7141 will automatically load the data from the serial memory without intervention from the host controller.

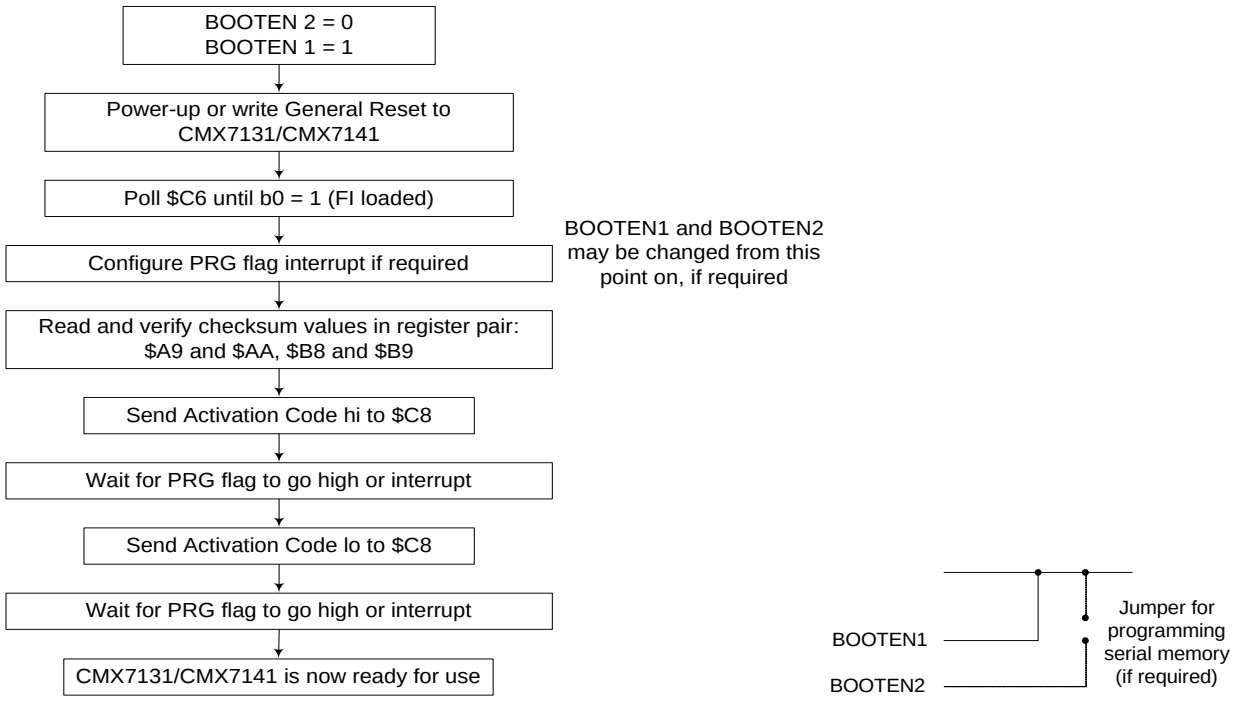


Figure 17 FI Loading from Serial Memory

The CMX7131/CMX7141 has been designed to function with Atmel AT25HP512 serial EEPROM and the AT25F512 flash EEPROM devices[2], however other manufacturers parts may also be suitable. The time taken to load the FI is dependent on the Xtal frequency; with a 6.144MHz Xtal, it should load in less than 1 second.

***NOTE**:FI loading from serial memory is not supported when FI-3.x is used in I/Q mode.*

[2] Note that these two memory devices have slightly different addressing schemes. FI-3 is compatible with both schemes.

6.4 NXDN Standard Vocoder Interface

For the NXDN standard vocoder all radio channel data will need to be transferred over the main C-BUS through the host. In this case the Vocoder 1 Enable Program registers (P1.11 and P1.12) should be set appropriately and the SPI-Codec ENA bit ($B1 bit 0) should be set to 1.

The connections for the NXDN standard vocoder are shown in Table 13.

Table 13 NXDN Standard Vocoder Connections

CMX7131/CMX7141 Pin:	AMBE-3000 Vocoder Device Pin:
SSOUT	SPI_STE
EPSI	SPI_RX_DATA
EPSO	SPI_TX_DATA
EPSCLK	SPI_CLK and SPI_CLK_IN.

6.4.1 Support for I²S Mode

The device can support I²S interfaces in mono, 16-bit mode only, for transmitting and receiving audio codec data using the SPI bus. This mode is selected in block 1 of the Programming register (see section 8.2.2). Figure 18 shows typical transmit waveforms.

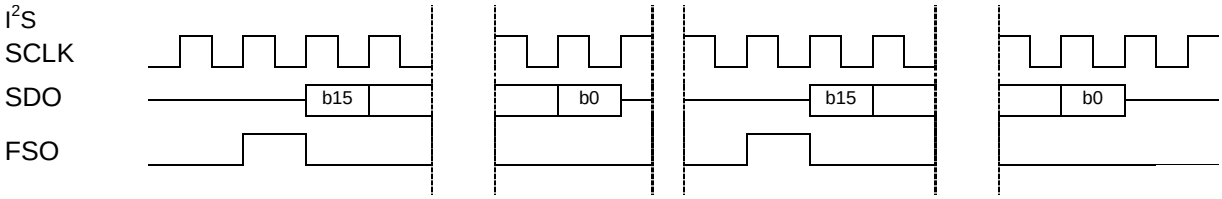


Figure 18 I²S Mode Support

6.5 Device Control

The CMX7131/CMX7141 can be set into the relevant mode to suit its environment. These modes are described in the following sections and are programmed over the C-BUS: either directly to operational registers or, for parameters that are not likely to change during operation, via the Programming register ($C8).

For basic operation:

(1) enable the relevant hardware sections via the Power Down Control register

(2) set the appropriate mode registers to the desired state

(3) select the required Signal Routing and Gain

(4) use the Modem Control register to place the device into Rx or Tx mode

To conserve power when the device is not actively processing a signal, place the device into IDLE mode. Additional power savings can be achieved by disabling any unused hardware blocks but care must be taken not to disturb any sections that are automatically controlled. Note that the BIAS block must be enabled to allow any of the input or output blocks to function.

See:

- Power Down Control - $C0 write
- Modem Control - $C1 write
- Modem Configuration - $C7 write.

6.5.1 General Notes

In normal operation, the most significant registers, in addition to the TxData and RxData blocks, are:

- Modem Control - $C1 write
- IRQ Status - $C6 read
- Analogue Output Gain - $B0 write
- Input Gain and Signal Routing - $B1 write
- TxAuxData Write - $C2 write
- Analogue Gain- $C3 write

Setting the Modem Mode to either Rx or Tx will automatically increase the internal clock speed to its operational speed and bring the device out of its powersave mode, whilst setting the Modem Mode to Idle will automatically return the internal clock to a lower (powersaving) speed. To access the Program Blocks (through the Programming register, $C8) the device MUST be in Idle mode.

Under normal circumstances the CMX7131/CMX7141 manages the main clock control automatically, using the default values loaded in Program Block 3.

6.5.2 Interrupt Operation

The CMX7131/CMX7141 will issue an interrupt on the IRQN line when the IRQ bit (bit 15) of the Status register and the IRQ Mask bit (bit 15) of the Interrupt Mask register are both set to 1. The IRQ bit is set when the state of the interrupt flag bits in the Status register change from a 0 to 1 and the corresponding mask bit(s) in the Interrupt Mask register is (are) set. Enabling an interrupt by setting a mask bit (0→1) after the corresponding Status register bit has already been set to 1 will also cause the IRQ bit to be set.

All interrupt flag bits in the Status register, except the PRG flag (bit 0), are cleared and the interrupt request is cleared following the command/address phase of a C-BUS read of the Status register. The PRG flag bit is set to 1 only when it is permissible to write a new word to the Programming register.

See:

- IRQ Status - $C6 read
- Interrupt Mask - $CE write

Continuous polling of the Status register ($C6) is not recommended due to both the increase in response time, host loading and potential digital noise generation due to bus activity. If the host cannot support a fully IRQ driven interface then it should route the IRQ signal to a host I/O pin and poll this pin instead.

6.5.3 Signal Routing

The CMX7131/CMX7141 offers a flexible routing architecture, with three signal inputs, a choice of two modulator configurations (to suit 2-point modulation or I/Q schemes) and a single audio output.

See:

- Input Gain and Signal Routing - $B1 write
- Modem Control - $C1 write
- Modem Configuration - $C7 write

The analogue gain/attenuation of each input and output can be set individually, with additional Fine Attenuation control available via the Program Blocks in the CMX7131/CMX7141. The Mic and Speaker gains are set by the vocoder. If the SPI-Codec mode is used, additional level control is available using the $B0 and $B1 registers.

See:

- Analogue Output Gain - $B0 write (Tx MOD1 and 2, Rx AUDIO)
- Input Gain and Signal Routing - $B1 write (Rx DISC input, Tx MIC, MOD1 and 2)
- Analogue Gain- $C3 write (Rx SPI/PCM Voice level).

In common with other FIs developed for the CMX7131/CMX7141, this device is equipped with two signal processing paths. However, in this implementation of the FI, Input 2 is ONLY used in SPI-Codec mode for the Tx audio input signal. Input 1 should be routed to one other of the three input sources (ALT, DISC or MIC) which should be connected to the radio's discriminator output. The internal signals Output 1 and 2 are used to provide either 2-point or I/Q signals and should be routed to the MOD1 and MOD2 pins as required. In I/Q mode Input 1 should be routed to the DISC input source for the I channel input and Input 2 should be routed to the ALT input source for the Q channel input.

It is important to correctly attach the signal from the CMX994 I/Q outputs to the CMX7141 DISC and ALT inputs. Crossing these connections will cause the CMX7141 dc offset calibration to fail, as attempted corrections to the I signal will be made to the Q signal and vice versa. Crossed connections can be swapped using the Input Gain and Signal Routing register ($B1:b5-2). Likewise, it is important that the sense of connection is correct between the CMX994 and CMX7141. If the input signals are inverted then attempts by the CMX7141 to remove the dc offset will, in fact, increase the dc offset. The inputs may be inverted by using the 'Input Invert' bit in the Analogue Output Gain register ($B0:b7). When demodulating the received signal (internally to the CMX7141), it is possible that the signal could be inverted, resulting in no framesync detection and, in effect, inverted data. Often this can be corrected by swapping the I and Q signals (changing the signal that leads in phase to the one that lags). However, the relationship between I/Q outputs of the CMX994 and the CMX7141 DISC and ALT inputs must be maintained as described above. Therefore the demodulated signal can be inverted using Programming Register block 0, P0.10 bit1 (IFD).

6.5.4 Modem Control

The CMX7131/CMX7141 operates in one of these operational modes:

- Idle
- Rx
- Tx
- CMX994 Pass-through
- Rx with CMX994 I/Q Cal.
- Rx with CMX994 I/Q Powersave.

At power-on or following a Reset, the device will automatically enter Idle mode, which allows for maximum powersaving whilst still retaining the capability of monitoring the AuxADC inputs (if enabled).
It is only possible to write to the Programming register whilst in Idle mode.

See:

- Modem Control - $C1 write

The RXENA and TXENA pins (GPIO1 and GPIO2) reflect bits 0 and 1 of the Modem Control register, as shown in Table 14. These can be used to drive external hardware without the host having to intervene. There are also two additional GPIO pins that are programmable under host control.

Table 14 Modem Mode Selection

Modem Control ($C1: b3-0)	Modem Mode	TXENA	RXENA
0000	Idle – low power mode	1	1
0001	Rx mode	1	0
0010	Tx mode	0	1
0011	*reserved*	x	x
0100	CMX994 Pass-through	1	1
0101	Rx with CMX994 I/Q cal (I/Q mode only)	1	0
1001	Rx with CMX994 Powersave (I/Q mode only)	1	0
others	*reserved*	x	x

The CMX994 Pass-through mode is used to control and monitor the CMX994 directly. This cannot be accessed if the CMX7131/CMX7141 is in Rx or Tx modes. Note the logic sense of RXENA and TXENA may be inverted by setting $A7:b1.

Table 15 Modem Control Selection

4-FSK Modem Control ($C1: b7-4)	Rx	Tx
0000	Rx Idle	Tx Idle
0001	Rx NXDN Formatted	Tx NXDN Formatted
0010	Rx NXDN Raw	*reserved*
0011	Rx 4-FSK EYE	Tx 4-FSK PRBS
0100	Rx Pass-through Mode	Tx 4-FSK Preamble
0101	*reserved*	Tx 4-FSK Mod set-up
0110	Sync	Tx Repeated Word
0111	Reset/Abort	Reset/Abort
1xxx	*reserved*	*reserved*

The Modem Mode bits and the Modem Control bits should be set together in the same C-BUS write.

6.5.5 Tx Mode NXDN Formatted

In Tx mode, the CMX7131/CMX7141 operates in NXDN formatted mode. The first block of control channel or payload data should be loaded into the C-BUS TxData registers before executing the mode change. A “DataReady” IRQ will be asserted when the registers have been read by the CMX7131/CMX7141 and the host can then supply further blocks of payload data. When all payload has been transmitted the CMX7131/CMX7141 will issue a “TxDone” IRQ and the host can then reset the Mode bits to either Rx or IDLE as required.

6.5.6 Tx Mode

In Tx mode operation ($C1, Modem Control = $0012), the Preamble sequence is automatically transmitted first, unless disabled by setting $C7:b11. The SW sequence is then automatically transmitted for each frame, followed by control channel and then payload data from the TxData registers. This continues until a data underflow condition occurs, the “End” frame is detected or the Mode is changed back to Rx or IDLE. LICH/SACCH blocks for the first frame should be loaded into the TxData registers before executing the Modem Mode change to Tx. The CMX7131/CMX7141 performs all necessary data scrambling, interleaving and FEC coding functions for the control channel and payload fields.

As soon as each control channel or payload data block has been read from the C-BUS TxData registers, the “DataReady” IRQ will be asserted and the next block of data may then be loaded. Note that payload data is always transmitted msb (most significant bit) first.

At the end of the call, the host should load control channel fields for the final frame with the SACCH “Message Classification” field set to “Idle”, and the FACCH1 “Message Classification” field set to “Clearing”. The CMX7131/CMX7141 will issue a “TxDone” IRQ when the frame has been sent and the host can then safely place the device into IDLE mode ($C1, Modem Control = $0000).

A typical host Tx sequence is:

1. Load TxData registers with LICH (7 bits) and SACCH (26 bits) for “Idle”
2. Set Modem Control = TxFormat, Modem Mode = Tx

   (Device will start transmission of Preamble and SW followed by contents of TxData registers)
3. Wait for DataReady IRQ
4. Load TxData registers with first part of FACCH1 (40 bits)
5. Wait for DataReady IRQ
6. Load TxData registers with second part of FACCH1 (40 bits)
7. Wait for DataReady IRQ
8. Load TxData registers with first part of FACCH1 (40 bits)
9. Wait for DataReady IRQ
10. Load TxData registers with second part of FACCH1 (40 bits)
11. Wait for DataReady IRQ
12. Load TxData registers with LICH (7 bits) and SACCH (26 bits) for “Audio”
13. Wait for DataReady IRQ
14. Load TxData registers with TCH data (72 bits)
15. Wait for DataReady IRQ
16. Load TxData registers with TCH data (72 bits)
17. Wait for DataReady IRQ
18. Load TxData registers with TCH data (72 bits)
19. Wait for DataReady IRQ
20. Load TxData registers with TCH data (72 bits)
21. Wait for DataReady IRQ
22. …repeat from 12 with the SACCH data set appropriately
23. Load TxData registers with LICH (7 bits) and SACCH (26 bits) for “Clearing”

24. Wait for DataReady IRQ
25. Load TxData registers with FACCH1 data (40 bits)
26. Wait for DataReady IRQ
27. Load TxData registers with FACCH1 data (40 bits)
28. Wait for DataReady IRQ.
29. Load TxData registers with FACCH1 data (40 bits)
30. Wait for DataReady IRQ
31. Load TxData registers with FACCH1 data (40 bits)
32. Wait for DataReady IRQ.

After the last data bit has left the modulator a “TxDone” IRQ will be asserted. At this point it is now safe for the host to change the Modem Control and Modem Mode to IDLE ($C1, Modem Control = $0000) and turn the RF transmitter off.

A typical host Tx sequence for Data Communications is:

1. Load TxData registers with LICH (7 bits) for “10 01 11 0”
2. Set Modem Control = TxFormat, Modem Mode = Tx
3. (Device will start transmission of Preamble and SW followed by contents of TxData registers)
4. Wait for DataReady IRQ
5. Load TxData registers with first part of UDCH1 (72 bits) – this includes the SU field
6. Wait for DataReady IRQ
7. Load TxData registers with second part of UDCH1 (72 bits)
8. Wait for DataReady IRQ
9. Load TxData registers with third part of UDCH1 (40 bits)
10. Wait for DataReady IRQ
11. Load TxData registers with LICH (7 bits) for “10 01 11 0”
12. …repeat from 4
13. Load TxData registers with LICH (7 bits) for “10 01 01 0”
14. Wait for DataReady IRQ
15. Load TxData registers with FACCH2 data (72 bits)
16. Wait for DataReady IRQ
17. Load TxData registers with FACCH2 data (72 bits)
18. Wait for DataReady IRQ.
19. Load TxData registers with FACCH2 data (40 bits)
20. Wait for DataReady IRQ

After the last data bit has left the modulator a “TxDone” IRQ will be asserted. At this point it is now safe for the host to change the Modem Control and Modem Mode to IDLE ($C1, Modem Control = $0000) and turn the RF transmitter off.

A typical host Tx sequence for Data Burst is:

1. Load TxData registers with LICH (7 bits) for “10 11 11 0”
2. Set Modem Control = TxFormat, Modem Mode = Tx
3. (Device will start transmission of Preamble and SW followed by contents of TxData registers)
4. Wait for DataReady IRQ
5. Load TxData registers with first part of UDCH2 (72 bits) – this includes the SU field
6. Wait for DataReady IRQ
7. Load TxData registers with second part of UDCH2 (72 bits)
8. Wait for DataReady IRQ
9. Load TxData registers with third part of UDCH1 (72 bits)
10. Wait for DataReady IRQ
11. Load TxData registers with fourth part of UDCH2 data (36 bits + 4 bits padding)
12. Wait for DataReady IRQ

After the last data bit has left the modulator a “TxDone” IRQ will be asserted. At this point it is now safe for the host to change the Modem Control and Modem Mode to IDLE ($C1, Modem Control = $0000) and turn the RF transmitter off.

The device will attempt to identify the end of the data burst by the contents of the burst, however the host can also inform the device directly by using the Block ID value of 00_2 on the final data transfer. This will automatically terminate the transmission once the final symbol of the data has been transmitted, and inhibit any “Tx Underrun” indication.

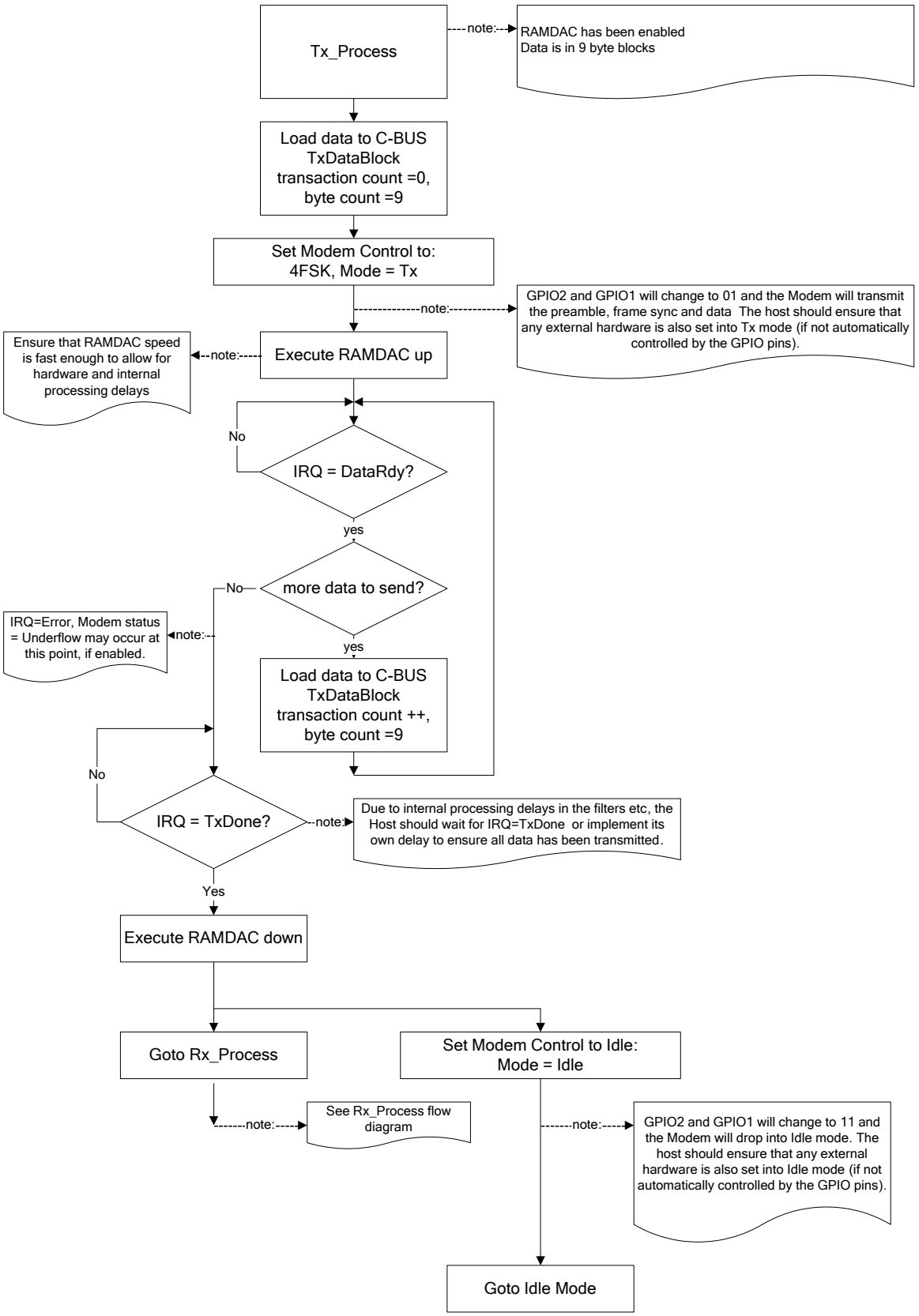


Figure 19 Tx Data Flow

6.5.7 Tx Mode PRBS

In PRBS mode ($C1, Modem Control = $0032) the preamble and frame sync are transmitted automatically followed by a PRBS pattern conforming to ITU-T O.153 (para. 2.1) giving a 511-bit repeating sequence.

6.5.8 Tx Mode Preamble

In Preamble mode ($C1, Modem Control = $0042) the preamble sequence [+3 +3 -3 -3] is sent continually. This can be used to set up and adjust the RF hardware.

6.5.9 Tx Mode Mod Set-up

In Mod Set-up mode ($C1 = $0052) the output depends on the selected Tx modulation type. In two-point mode, a repeating sequence of eight +3 symbols followed by eight -3 symbols is sent, and in I/Q mode a continuous sequence of +3 symbols is sent. This can be used to set up and adjust the RF hardware.

6.5.10 Tx Mode Repeated Word

In Repeated Word mode ($C1 = $0062) the preamble and frame sync are transmitted automatically followed by the data provided by the host in TxData4. This feature allows the NXDN standard test waveforms to be transmitted as part of the test and qualification procedures.

6.5.11 Tx Sequencer

The Tx Sequencer provides an automated way of executing a sequence of actions, thus reducing timing constraints placed on the host. It is controlled by setting b15 in the Modem Configuration register ($C7) to 1. If enabled, it will automatically start executing its sequence of transmit actions when the CMX7131/CMX7141 is placed in Tx mode. The timing values for each action can be set in P3.75 to P3.79 and are defined in increments of 250µs.

The duration of the ramp by the RAMDAC is controlled by P3.80 – The RAMDAC scan time configuration. It can be configured to ramp over a period of between 80µs and 32ms.

On expiry of the Tx ENA inactive delay the CMX7131/CMX7141 will return to the previous operating mode automatically. It will also assert the “EndOfSequence” IRQ to the host at this point ($C6:b2 =1), signalling that the Tx sequence has completed.

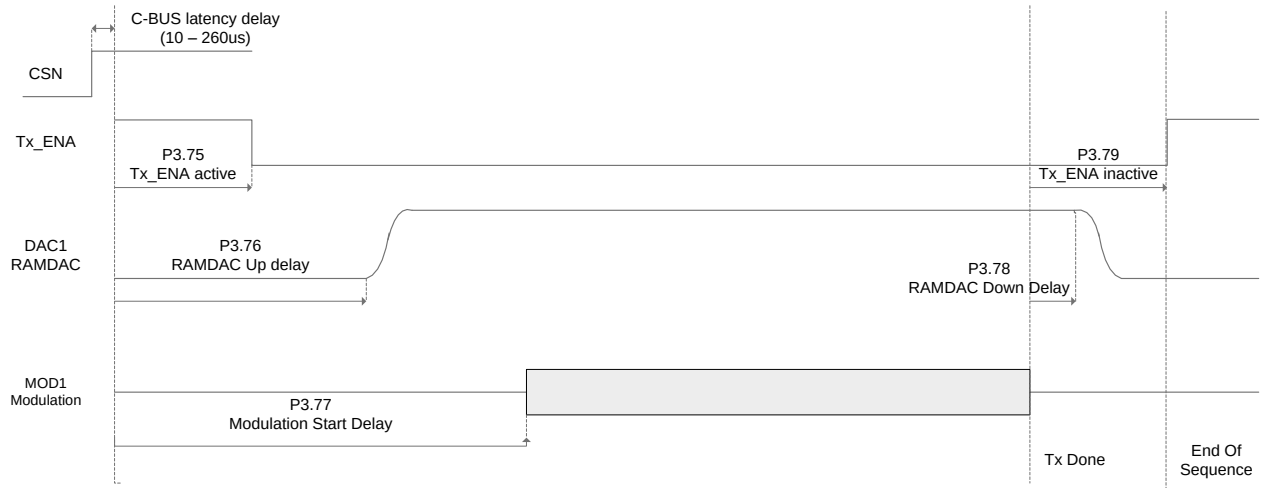


Figure 20 Automatic Tx Sequencer

6.5.12 Rx Mode NXDN Formatted

In Rx mode the received signal should be routed through Input1. In NXDN Raw and Formatted modes the CMX7131/CMX7141 will first search for frame synchronisation, and when this has been achieved the following data is demodulated and supplied to the host through the RxData registers. A “DataReady” IRQ indicates when each new block becomes available. The CMX7131/CMX7141 will continue demodulating the input signal until the host resets the Mode bits to Tx or IDLE, or the modem detects the end of a call and restarts the framesync search automatically.

6.5.13 Rx Mode Raw

Rx Mode Raw is included in this FI to facilitate BER measurements. In this mode ($C1, Modem Control = $0021), once a valid Frame Sync has been detected, all following data received is loaded directly into the C-BUS RxData registers. This continues until the end of the burst (even if there is no valid signal at the input). On exiting Rx Mode Raw, there may be a DataRdy IRQ pending which should be cleared by the host. Note that Raw Mode operation always requires the incoming data to be preceded with a valid Preamble and Frame Sync pattern in order to derive timing information for the demodulator. The device will update the C-BUS RxData registers with Rx payload data as it becomes available. The host MUST respond to the DataRDY IRQ before the RxData registers are over-written by subsequent data from the modem.

6.5.14 Rx Mode Eye

In Rx 4FSK EYE mode ($C1 = $0031), the filtered received signal is output at the MOD1 pin as an ‘eye’ diagram for test and alignment purposes. A trigger pulse is output at the MOD2 pin to allow viewing on a suitable oscilloscope. The trigger pulse is generated directly from the receiver xtal source, not from the input signal. In I/Q mode, this includes I/Q dc calculation in RXDATA0, RXDATA1 and computed Powersave Levels 1,2,3 in RXDATA2-4.

6.5.15 Rx Pass-through Mode

Rx Pass-through mode ($C1 = $0041) is very similar to Rx Mode Eye as described in section 6.5.14, however the output at the MOD1 pin is the flat, unfiltered signal. A trigger pulse is output at the MOD2 pin to allow viewing on a suitable oscilloscope. The trigger pulse is generated directly from the receiver xtal source, not from the input signal.

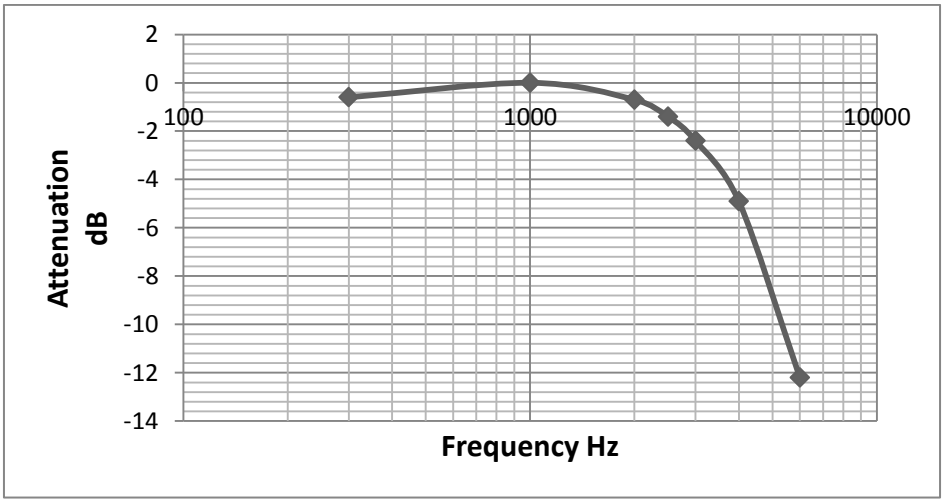


Figure 21 Frequency Response for Rx Pass-through Mode

6.5.16 Rx Mode with CMX994 AGC (I/Q Mode only)

By default, when receiving in I/Q Mode the CMX7131/CMX7141 will control its internal analogue gain and the gain of the CMX994 in order to keep the received I/Q signals within an acceptable dynamic range. This AGC feature may be disabled using Program Block P2.0 (I/Q AGC function), in which case any setup that the host has made of the CMX994 will determine its gain, with the input gain of the CMX7131/CMX7141 being controlled using the Input Gain and Signal Routing - $B1 write register.

It is important to ensure that the dc offset on the I/Q signals is small, otherwise the AGC function will interpret the dc as a large received signal and never select maximum gain. This problem can be addressed by calibrating the CMX994 as described in section 6.5.17.

6.5.17 Rx Mode with CMX994 I/Q Cal (I/Q Mode only)

When receiving, the CMX7131/CMX7141 will estimate and remove the dc error present in the I/Q signals from a CMX994 receiver. However, it is necessary to calibrate the CMX994 so that the magnitude of the dc offsets present is as small as possible. Selecting Rx mode with CMX994 I/Q Cal ($C1, Modem Control b3-0 = $5) causes the CMX7131/CMX7141 to measure the dc offset on the DISC and ALT input pins and to control the CMX994 receiver to minimise the dc offsets. The CMX7131/CMX7141 will then begin to receive normally – correcting the remaining dc offset internally.

Important note: when calibrating I/Q it is important that the I/Q signals are not swapped when interfacing to the CMX994. This can be corrected by using bits 2 to 5 of the Input Gain and Routing register ($B1).

If the CMX994 is poorly calibrated, a loss of headroom when receiving signals will result. In extreme cases, when large dc offsets are amplified, the result can be big enough to prevent the AGC from reaching maximum gain as it interprets the dc offset itself as a large signal.

Having calibrated the CMX994, the value written to the CMX994 Rx Offset register is available to read using the Aux Data and Status ($A9, $AA) registers. This means that having calibrated the CMX994 on a receive channel the calibration result may be stored by the host microcontroller and restored at a later time using CMX994 pass-through mode ($C1, Modem Control b3-0 = $4) to write the value directly to the CMX994 Rx Offset register as required.

6.5.18 Rx Mode with CMX994 Powersave (I/Q Mode only)

Selecting Rx with CMX994 Powersave mode ($C1, Modem Control b3-0 = $9) will cause the CMX7131/CMX7141 to control the CMX994, switching it into a low-power state for a short period of time. Once the powersave timer has expired then the CMX994 and the internal circuits of the CMX7131/CMX7141 will be powered-up, ready to receive.

On entering the powered-up state, the CMX7131/CMX7141 will monitor the received I/Q signals for energy in its sampled bandwidth and if there is no signal present it will return to the powersave state, powering down the CMX994. If sampled energy is found then the signal is passed through a channel filter and the resulting signal measured. If no signal is found the powersave state is selected once more, otherwise the powersave event IRQ is raised and the CMX994 and CMX7131/CMX7141 remain on and in receive mode, until the Modem Control register is re-written to reapply the powersave mode. This can be triggered by monitoring the RSSI once the powersave IRQ has been observed.

Throughout the time that the receiver is on, the CMX7131/CMX7141 will search for a frame sync and start receiving the data following that frame sync, if found. However, dependent on the powersave period, it is possible that the frame sync at the start of a burst may be missed, in which case ‘late entry’ is possible.

Thresholds for comparison and timings for powersave mode may be adjusted, potentially improving powersaving by being powered down for a greater period of time, but at the expense of a slower reaction to a received signal. See the Aux Config - $CD write register.

6.5.19 Reset/Abort

From each Rx or Tx mode, a Reset/Abort aborts the current state machine and drops into the corresponding (Rx or Tx) Idle mode. The only difference between this and going directly into the corresponding Idle mode is that all of the buffers and filters are flushed out first with Reset/Abort.

6.5.20 Data Transfer

Payload data is transferred from/to the host using blocks of five Rx and five Tx 16-bit C-BUS registers, allowing up to 72 bits (9 bytes) of data to be transferred in sequence. The lowest 8 bits of the register block are reserved for a Byte Counter, Block ID and a Transaction Counter. The byte count indicates how many bytes in the data block are valid and avoids the need to perform a full five word C-BUS read/write if only a smaller block of data need to be transferred. If a data transfer does not consist of an integer number of bytes, then the final byte transfer should be padded with zeroes up to the byte boundary.

Table 16 C-BUS Data Registers

C-BUS Address	Function	C-BUS Address	Function
$B5	Tx data 0-7 and info	$B8	Rx data 0-7 and info
$B6	Tx data 8-23	$B9	Rx data 8-23
$B7	Tx data 24-39	$BA	Rx data 24-39
$CA	Tx data 40-55	$BB	Rx data 40-55
$CB	Tx data 56-71	$C5	Rx data 56-71

The Block ID is ignored in Raw Data mode, but should be set to 01_2 (payload) for consistency with NXDN formatted mode (see User Manual section 8.1.17).

Bits 7 and 6 hold the Transaction Counter, which is incremented modulo 4 on every read/write of the Data Block to allow detection of data underflow and overflow conditions. In Tx mode the host must increment the counter on every write to the TxData block, and if the CMX7131/CMX7141 identifies that a block has been written out of sequence, the Event bit (C-BUS register $C6, b14) will be asserted and an IRQ raised, if enabled. The device detects that new data from the host is available by the change in the value of the Transaction Counter, therefore the host should ensure that all the data is available in the TxData block before updating this register (i.e. it should be the last register the host writes to in any block transfer). In Rx mode, the CMX7131/CMX7141 will automatically increment the counter every time it writes to the RxData block. If the host identifies that a block has been written out of sequence, then it is likely that a data overrun condition has occurred and some data has been lost. If a CRC failure has been detected when decoding the data block, an 'Event' IRQ is issued concurrently with the 'Data Ready' IRQ along with a status code in the Modem Status register ($C9).

6.5.21 CMX994 Pass-through Mode

To allow the host to communicate directly with the CMX994 for test and configuration purposes, a pass-through mode is available which allows any CMX994 C-BUS register to be written. This mode uses the TxData0, RxData0 and Programming registers on the CMX7131/CMX7141.

To write to the CMX994:

- Set the CMX7131/CMX7141 to CMX994 Pass-through mode ($C1=$0004)
- Wait for the Program Flag to be set ($C6 b0)
- Write the CMX994 data value to the TxData0 register ($B5)
- Write the CMX994 C-BUS address to the Programming register ($C8) with b15-13=$011_2$
- Wait for the Program Flag to be set ($C6 b0).

6.6 NXDN Mode Operation

The CMX7131/CMX7141 performs all frame building/splitting and FEC coding/decoding, which relieves the host controller of a significant processing load. During voice calls voice is transferred to and from the vocoder under host control. In Rx mode the CMX7131/CMX7141 monitors the incoming control channel fields and will only accept calls if the programmed address requirements are satisfied. This allows the host to remain in a power-down or “sleep” state until it is really necessary to wake up, enhancing the battery life of the final product design.

6.6.1 Frame Format

NXDN calls contain an optional preamble sequence (controlled by $C7:b11) followed by a continuous stream of 384-bit (80ms) frames. Three frame formats are defined by the standard: “Audio Communications Format”, “Data Communications Format” and “Data Communications Burst Format”.

All frames start with a 20-bit Sync Word followed by a 16-bit Link Information Channel (LICH) block. The LICH fields indicate the frame format and payload type, and the CMX7131/CMX7141 uses this information to determine how to process each frame in both Tx and Rx. The “Communications mode identification” field sets the frame format and the “Option” field sets the payload field type (TCH, FACCH1, FACCH2, UDCH1).

In an “Audio Communications Format” call the 60-bit Slow Associated Control Channel (SACCH) block is present in all frames. The “Start” and “End” frames carry two 144-bit “Fast Associated Control Channel 1” (FACCH1) blocks in the payload fields instead of Traffic Channel (TCH) data. The CMX7131/CMX7141 scans the “SU” and “Message Classification” fields contained in the SACCH and FACCH1 blocks and uses these to perform address matching (in Rx mode) and to decide whether to route the following TCH data via the host or to enable audio sample routing when in SPI-CODEC mode. The CMX7131/CMX7141 also checks the “Message Classification” field for the “Clearing” value which indicates an “End” frame. When this is found the CMX7131/CMX7141 terminates call processing.

Note that in an “Audio Communications Format” call the TCH bearing frames are grouped into superframes, in which the information contained in SACCH may be split across four consecutive frames. Dis-assembly and re-assembly of the contents must be done by the transmitting and receiving hosts; this function is not performed by the CMX7131/CMX7141.

Note that all block sizes given above refer to “over-air” bits, some of which are FEC coded. Because the CMX7131/CMX7141 performs all FEC coding functions, the block sizes of data transfers between the CMX7131/CMX7141 and host are smaller in most cases except for uncoded TCH blocks.

Table 17 RxData 0/TxData 0 Block ID settings

RxData 0 TxData 0 b5-4	Block ID
00	Final Payload Data (Tx only)
01	Normal Payload Data
10	LICH
11	SACCH and LICH

LICH Data:
The TxData block is interpreted in the following manner:

TxData	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	LICH0-6							Count		1	0	0	0	0	1
1	Not used															
2	Not used															
3	Not used															
4	Not used															

	6	5	4	3	2	1	0
LICH	RF Channel Type		Functional Channel Type		Option		Dir

Conventional Mode LICH processing:

RF	RF Channel Type
00	*reserved*
01	*reserved*
10	Direct Communication
11	*reserved*

D	Direction
0	Uplink or MS - MS
1	Downlink

F	O	Mode	Payload content
00	**00**	Audio Communication, non-superframe SACCH follows	**FACCH1 / FACCH1**
00	01		*reserved FACCH1 / FACCH1*
00	10		*reserved FACCH1 / FACCH1*
00	11		*reserved FACCH1 / FACCH1*
01	**00**	Data Communication	**FACCH2**
01	01		*reserved FACCH2*
01	10		*reserved UDCH1*
01	**11**		**UDCH1**
10	**00**	Audio Communication, superframe SACCH follows	**FACCH1 / FACCH1**
10	01		FACCH1 / TCH
10	10		TCH / FACCH1
10	**11**		**TCH / TCH**
11	00	Data Burst	*reserved FACCH1 / FACCH1*
11	01		*reserved FACCH1 / TCH*
11	10		*reserved TCH / FACCH1*
11	11		*reserved TCH / TCH*

Examples:

Start frame:	10 00 00 0	Audio with FACCH1 (single frame)
TCH frame:	10 10 11 0	Audio with TCH payload (super-frame)
Clearing frame:	10 00 00 0	Audio with FACCH1 (single frame)

Class-D Trunking Mode LICH processing:

RF	RF Channel Type
00	*reserved*
01	*reserved*
10	*reserved*
11	**RTCH2**

D	Direction
0	Uplink / Inbound
1	Downlink / Outbound

F	O	Mode	Payload content
00	**00**	Audio Communication, non-superframe SACCH follows	**FACCH1 / FACCH1**
00	**01**		**FACCH1 + G**
00	10		*reserved FACCH1 / FACCH1*
00	11		*reserved FACCH1 + G*
01	**00**	Data Communication	**FACCH3**
01	01		*reserved FACCH3*
01	10		*reserved UDCH2*
01	**11**		**UDCH2**
10	**00**	Audio Communication, superframe SACCH follows	**FACCH1 / FACCH1**
10	01		FACCH1 / TCH
10	10		TCH / FACCH1
10	**11**		**TCH / TCH**
11	00	Data Burst	*reserved FACCH1 / FACCH1*
11	01		*reserved FACCH1 / TCH*
11	10		*reserved TCH1/ FACCH1*
11	11		*reserved TCH / TCH*

Note: In Rx mode the LICH data is protected by di-bit encoding and a single parity bit. In poor signal conditions, it may not be possible to determine if this data has been received with one or more errors. The LICH decoder will attempt to verify the LICH data by using the knowledge that the RF field must be a fixed value for Conventional (10_2) or Class-D (11_2) modes and whether or not the SACCH data (which is protected by a CRC) indicates if a superframe is in progress or not.
The tables also include the actions that will be taken should the "*reserved*" conditions be encountered. It is up to the host to decide whether to discard these bursts or not.

LICH and SACCH Data:
The TxData/RxData block is interpreted in the following manner:

TxData RxData	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	LICH 0-6							Count		1	1	0	1	0	1
1	SACCH 0-7								SACCH 8-15							
2	SACCH 16-23								0	0	0	0	0	0	SACCH 24-25	
3	Not used															
4	Not used															

TCH Payload Data:
See Table 17 and User Manual section 8.1.11.

6.6.2 Addressing

The NXDN standard allows individual or group addressing systems to be implemented using the 6-bit "RAN" field in the SACCH block. The host can load six RAN codes into Program Block 1 as "Own-RANs" and the CMX7131/CMX7141 will only accept an incoming call if one of these is matched or if the "All-Call" RAN (all-zeros) is received. If the "Open Rx" bit is set in the Modem Control register ($C7), all decoded over-air is delivered to the host over the C-BUS. The CMX7131/CMX7141 can also be programmed to accept or reject calls depending on the value of the SACCH "Message Classification" field, using the Manufacturer ID in Program Block 1.

6.6.3 Rx Mode

In Rx mode ($C1, Modem Control = $0011), the CMX7131/CMX7141 automatically starts searching for frame synchronisation. When a valid framesync sequence is detected, an "FS1 Detect" or "FS2 Detect" IRQ is asserted and the data demodulator is enabled. The CMX7131/CMX7141 then processes the first frame to extract control channel data and decide whether to accept the call. The CMX7131/CMX7141 performs all the necessary data de-scrambling, de-interleaving and FEC decoding functions for control channel and payload data blocks. If the LICH or SACCH control channel blocks in the first frame fail their CRC or parity-bit checks, the CMX7131/CMX7141 will continue scanning incoming frames until valid control channel information is received.

The SACCH/FACCH1 "RAN" in the "SU" field is then checked and accepted if either:

(a) it is the all-zeros "All-Call" RAN, or

(b) it matches one of the device's "RAN" programmed by the host into Program Block P1.0 to P1.5.

If this check fails, and the "Open Rx" bit is clear, the call is rejected and the CMX7131/CMX7141 restarts framesync search automatically without host intervention.

Otherwise, the call is accepted, a "Called" IRQ is issued to the host and the User Code and ID match-type (exact match or All-Call) are reported in the RxAuxData register ($CC), and the CMX7131/CMX7141 then begins transferring data blocks to the host.

Control channel fields and payload data blocks are transferred via the RxData registers. The Block ID field in the RxData0 register informs the host what type of data block each transfer contains. The host MUST respond to each "DataReady" IRQ before the RxData registers are overwritten by subsequent data blocks. If "soft" data mode has been selected, uncoded payload data is transferred in 4-bit log-likelihood-ratio (LLR) format and in this mode the host must be able to service the "DataReady" IRQs and RxData registers at four times the normal rate to avoid loss of data.

When a CRC or parity-bit failure has been detected in a control channel or payload data block, an additional "Event" IRQ is issued to the host at the same time as the "DataReady" IRQ, with a corresponding error code in the Modem Status register, $C9.

Received frames are processed continually until an "End" frame is detected, the Call Drop Threshold is exceeded (P0.0) or the Mode is changed back to IDLE. The CMX7131/CMX7141 will then automatically disable the SPI-CODEC (if enabled), transfer the contents of the final frame to the host, and restart framesync search automatically unless switched to IDLE.

See:

- RxData 0 - $B8 read
- RxAuxData Read - $CC read.

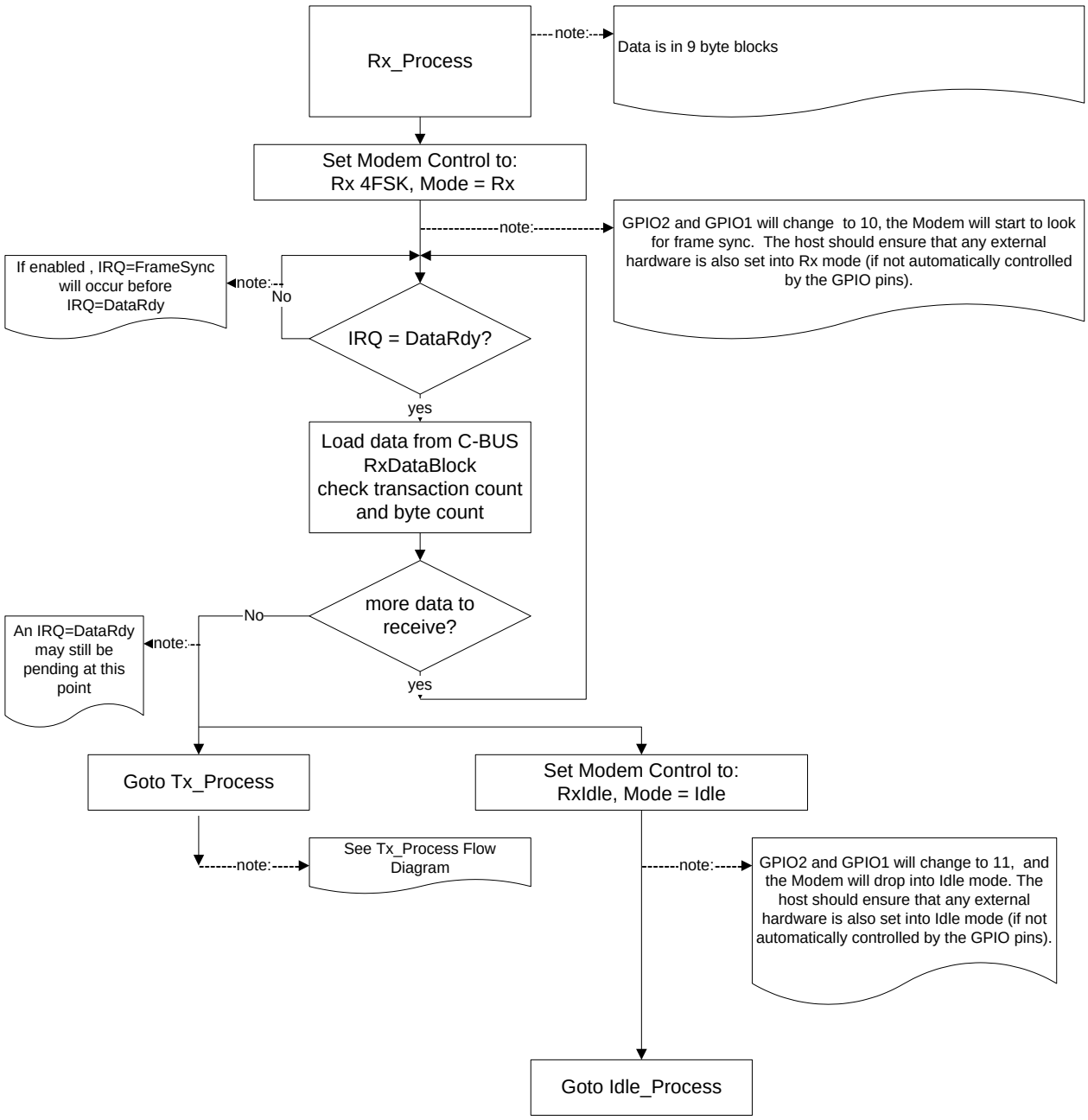


Figure 22 Rx Data Flow

6.7 Squelch Operation

Many Limiter/Discriminator chips provide a noise-quieting squelch circuit around an op-amp configured as a filter. This signal is conventionally passed to a comparator to provide a digital squelch signal, which can be routed directly to one of the CMX7131/CMX7141's GPIO pins or to the host. However with the CMX7131/CMX7141, the comparator and threshold operations can be carried out by one of the AuxADCs with programmable thresholds and hysteresis functions.

See:

- IRQ Status - $C6 read
- AuxADC Configuration - $A7 write

Note that the delays inherent in the squelch detection filter and detector may make its use problematic in a data-centric radio system.

6.8 GPIO Pin Operation

The CMX7131/CMX7141 provides four GPIO pins: GPIO1, GPIO2, GPIOA and GPIOB. RXENA (GPIO1) and TXENA (GPIO2) are configured to reflect the Tx/Rx state of the Mode register (TXENA and RXENA, active low).

See:

- Modem Control - $C1 write

Note that TXENA and RXENA will not change state until the relevant mode change has been executed by the CMX7131/CMX7141. This is to allow the host sufficient time to load the relevant data buffers and the CMX7131/CMX7141 time to encode the data required prior to its transmission. There is thus a fixed time delay between the GPIO pins changing state and the data signal appearing at the MOD output pins.

During the power-on sequence (until the FI has completed its load sequence) these pins have only a weak pull-up applied to them so care should be taken to ensure that any loading during this period does not adversely affect the operation of the unit.

GPIOA and GPIOB are host programmable for input or output using the AuxADC Configuration register, $A7. The default state is input, with a weak pullup resistor. When set for input the values can be read back using the Modem Status register, $C9.

The TXENA and RXENA pins may optionally be set to active high operation by setting bit 1 of register $A7 to 1 (the same bit affects both pins). When using this feature please note that following initial boot or a reload of the function image, the pins will be reset to the default (active low) state. Care should be taken with any attached devices which might consider the signal as active until the $A7 register can be written to.

6.9 Auxiliary ADC Operation

The inputs to the two auxiliary ADCs can be independently routed from any of the signal input pins under control of the Signal Routing register, $A7. Conversions will be performed as long as a valid input source is selected, to stop the ADCs, the input source should be set to “off”. Register $C0, b6, BIAS, must be enabled for auxiliary ADC operation.

Averaging can be applied to the AuxADC readings by selecting the relevant bits in the AuxADC configuration register, $A7, the length of the averaging is determined by the value in the Program Block (P3.0 and P3.1), and defaults to a value of 0. This is a rolling average system such that a proportion of the current data will be added to the last average value. The proportion is determined by the value of the average counter in P3.0 and P3.1.

For an average value of:

0 = 50% of the current value will be added to 50% of the last average value,

1 = 25% of the current value will be added to 75% of the last average value,

2 = 12.5% etc.

The maximum useful value of this field is 7.

High and low thresholds may be independently applied to both AuxADC channels (the comparison is applied after averaging, if this is enabled) and an IRQ generated when a rising edge passes the high threshold or a falling edge passes the low threshold, see Figure 23 and AuxADC Configuration - $A7 write register. The thresholds are programmed via the Aux Config - $CD write register.

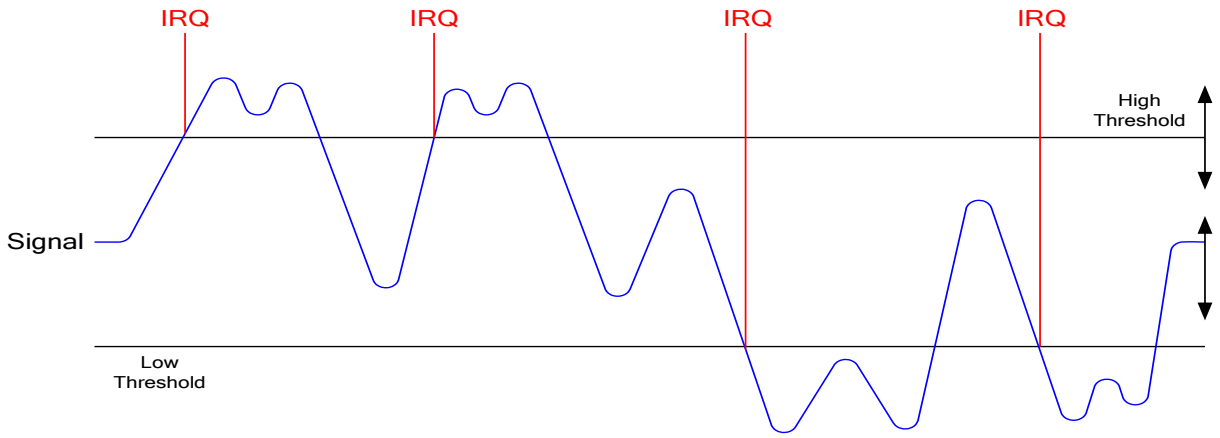


Figure 23 AuxADC IRQ Operation

Auxiliary ADC data is read back in the AuxADC Data registers ($A9 and $AA) and includes the threshold status as well as the actual conversion data (subject to averaging, if enabled).

See:

- AuxADC Configuration - $A7 write
- AuxADC1 Data and Threshold Status - $A9 read
- AuxADC2 Data and Threshold Status - $AA read
- Aux Config - $CD write

6.10 Auxiliary DAC/RAMDAC Operation

The four auxiliary DAC channels are programmed via the AuxDAC Control register, $A8. AuxDAC channel 1 may also be programmed to operate as a RAMDAC which will automatically output a pre-programmed profile at a programmed rate. The AuxDAC Control register, $A8, with b12 set, controls this

mode of operation. The default profile is a raised cosine (see Table 21), but this may be over-written with a user- defined profile by writing to Programming register P3.11. The RAMDAC operation is only available in Tx mode and, to avoid glitches in the ramp profile, it is important not to change to Idle or Rx mode whilst the RAMDAC is still ramping. The AuxDAC outputs hold the user-programmed level during a powersave operation if left enabled, otherwise they will return to zero. Note that access to all four AuxDACs is controlled by the AuxDAC Control register, $A8, and therefore to update all AuxDACs requires four writes to this register. It is not possible to simultaneously update all four AuxDACs.

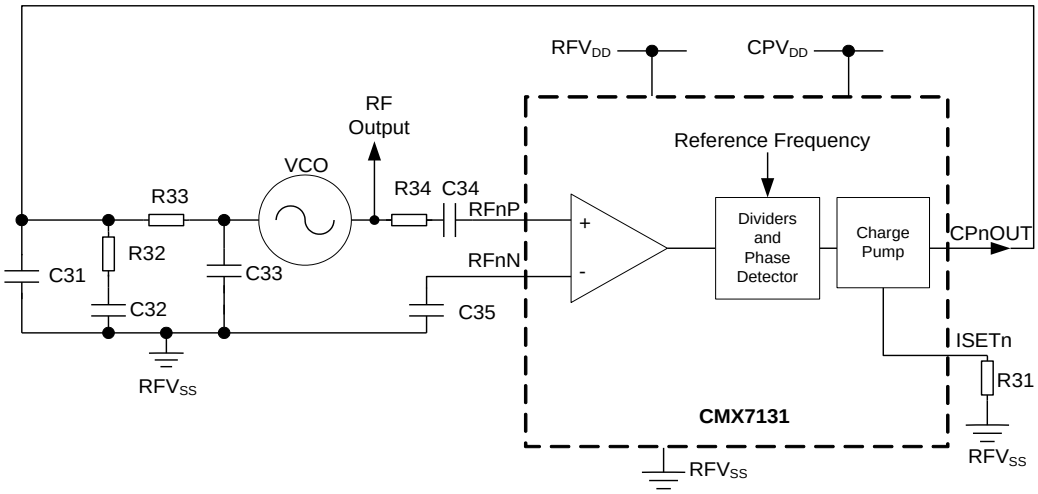
See:
- AuxDAC Data and Control - $A8 write

6.11 RF Synthesiser (CMX7131 only)

The CMX7131 includes two Integer-N RF synthesisers, each comprising a divider, phase comparator and charge pump. The divider has two sets of N and R registers: one set can be used for transmit and the other for receive. The division ratios can be set up in advance by means of C-BUS registers. A single C-BUS command will change over from the transmit to the receive division ratios, or vice versa, enabling a fast turnaround.

See:
- RF Synthesiser Data (CMX7131 only) - $B2 write
- RF Synthesiser Control (CMX7131 only) - $B3 write
- RF Synthesiser Status (CMX7131 only) - $B4 8-bit read

External RF components are needed to complete the synthesiser circuit. A typical schematic for a 446MHz synthesiser (3.125kHz comparison frequency) is shown in Figure 24.



Note: n = 1 or 2 for Synthesiser 1 or 2

Figure 24 Example RF Synthesiser Components

R31	0Ω	C31	22nF
R32	5.6kΩ	C32	470nF
R33	10kΩ	C33	10nF
R34	100Ω	C34	1nF
		C35	1nF

Resistors ±5%, capacitors and inductors ±20% unless otherwise stated.

Note: R31 is chosen within the range 0Ω to 30kΩ and selects the nominal charge pump current.

It is recommended that C34 and C35 be kept close to the VCO and that the stub from the VCO to the CMX7131 be kept as short as possible. The loop filter components should be placed close to the VCO.

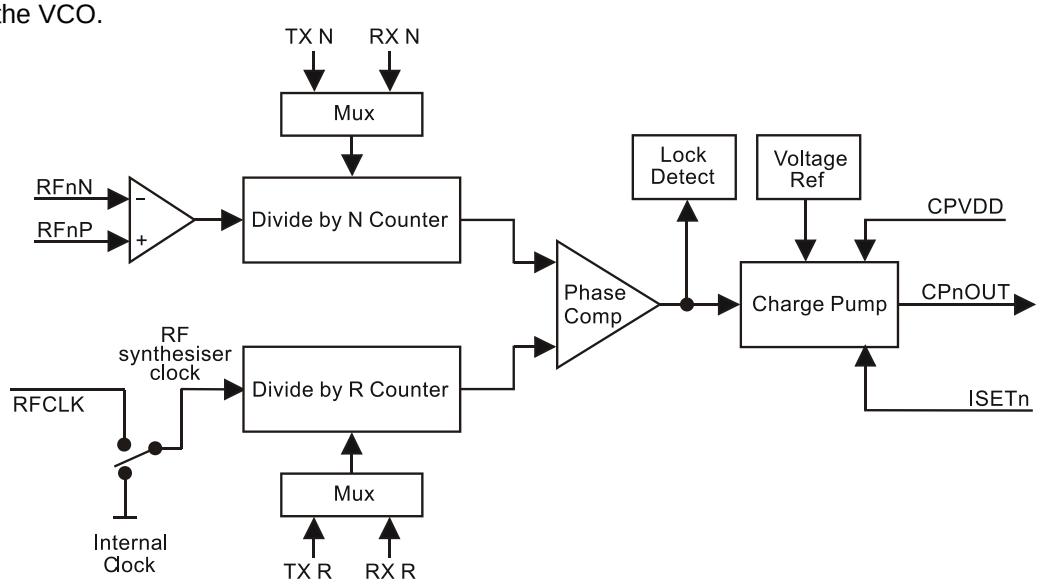


Figure 25 Single RF Synthesiser Block Diagram

The two RF synthesisers are programmable to any frequency in the range 100MHz to 600MHz. Figure 25 is a block diagram of one synthesiser channel. The RF synthesiser clock is selectable between the XTAL/CLK input or the clock supplied to the RFCLK input pin. The RF synthesiser clock is common to both channels. The charge pump supply pin CPVDD and the RF synthesiser power supply pins RFVSS and RFVDD are also common to both channels. The remaining pins are designated with a 1 or 2 to indicate to which RF synthesiser block they belong. The N and R values for Tx and Rx modes are channel specific and can be set from the host µC via the C-BUS. Various channel specific status signals are also accessible via C-BUS. The divide by N counter is 20 bits; the R counter is 13 bits. Typical external components are shown in Figure 24.

Both synthesisers are phase locked loops (PLLs) of the same design, utilising external VCOs and loop filters. The VCOs need to have good phase noise performance although it is likely that the high division ratios used will result in the dominant noise source being the reference oscillator. The phase detectors are of the phase-frequency type with a high impedance charge pump output requiring just passive components in the loop filter. Lock detect functions are built in to each synthesiser and the status reported via C-BUS. A transition to out-of-lock can be detected and communicated via a C-BUS interrupt to the host µC. This can be important in ensuring that the transmitter cannot transmit in the event of a fault condition arising.

Two levels of charge pump gain are available to the user, to facilitate the possibility of locking at different rates under program control. A current setting resistor (R31) is connected between the ISET pin (one for each PLL system) and the respective RFV_{SS}. This resistor will have an internally generated band gap voltage expressed across it and may have a value of 0Ω to 30kΩ, which (in conjunction with the on-chip series resistor of 9.6kΩ) will give charge pump current settings over a range of 2.5mA down to 230µA (including the control bit variation of 4 to 1). The value of the current setting resistor (R31) is determined in accordance with the following formulae:

Gain bit set to 1: R31 (in Ω) = (24/Icp) – 9600
Gain bit cleared to 0: R31 (in Ω) = (6/Icp) – 9600
Where Icp is the charge pump current (in mA)

Note that the charge pump current should always be set to at least 230µA. The ‘gain bit’ refers to either bit 3 or bit 11 in the RF Channel Control register, $B3.

The step size (comparison frequency) is programmable; to minimise the effects of phase noise this should be kept as high as possible. This can be set as low as 2.5kHz (for a reference input of 20MHz or less), or up to 200kHz – limited only by the performance of the phase comparator.

The frequency for each synthesiser is set by using two registers: an ‘R’ register that sets the division value of the input reference frequency to the comparison frequency (step size), and an ‘N’ register that sets the division of the required synthesised frequency from the external VCO to the comparison frequency. This yields the required synthesised frequency (Fs), such that:

$$Fs = (N / R) \times F_{REF}$$ where F_{REF} is the selected reference frequency.

Other parameters for the synthesisers are the charge pump setting (high or low).

Since the set-up for the PLLs takes 4 x “RF Channel Data register” writes it follows that, while updating the PLL settings, the registers may contain unwanted or intermediate values of bits. These will persist until the last register is written. It is intended that users should change the content of the “RF Channel Data register” on a PLL that is disabled, powersaved or selected to work from the alternate register set (“Tx” and “Rx” are alternate register sets). There are no interlocks to enforce this intention. The names “Tx” and “Rx” are arbitrary and may be assigned to other functions as required. They are independent sets of registers, one of which is selected to command each PLL by changing the settings in the RF Synthesiser Control (CMX7131 only) - $B3 write register.

For optimum performance, a common master clock should be used for the RF synthesisers (RFClock) and the baseband sections (Main and Auxiliary System Clocks). Using unsynchronised clocks can result in spurious products being generated in the synthesiser output and in some cases difficulty may be experienced with obtaining lock in the RF synthesisers.

Lock Status

The lock status can be observed by reading the RF Channel Status register, $B4, and the individual lock status bits can (subject to masking) provide a C-BUS interrupt.

The lock detector can use a tolerance of one cycle or four cycles of the reference clock (not the divided version that is used as a comparison frequency) in order to judge phase lock. An internal shift register holds the last three lock status measurements and the lock status bits are flagged according to a majority vote of these previous three states. Hence, one occasional lock error will not flag a lock fail. At least two successive phase lock events are required for the lock status to be true. Note that the lock status bits confirm phase lock to the measured tolerance and not frequency lock. The synthesiser may take more time to confirm phase lock with the lock status bits than the time to switch from channel to channel. The purpose of a 4-cycle tolerance is for the case where a high frequency reference oscillator would not tolerate a small phase error.

RF Inputs

The RF inputs are differential and self-biased (when not powersaved). They are intended to be capacitively coupled to the RF signal. The signal should be in the range 0dBm to –20dBm (not necessarily balanced). To ensure an accurate input signal the RF should be terminated with 50Ω as close to the chip as possible and with the “N” and “P” inputs capacitively coupled to the input and ground, keeping these connections as short as possible. The RF input impedance is almost purely capacitive and is dominated by package and printed circuit board parasitics.

Guidelines for Using the RF Synthesisers

- RF input slew rate (dv/dt) should be 14V/µs minimum
- The RF synthesiser 2.5V digital supply can be powered from the VDEC output pin
- RF clock sources and other, different clock sources must not share common IC components, as this may introduce coupling into the RF. Unused ac-coupled clock buffer circuits should be tied off to a dc supply, to prevent them oscillating
- It is recommended that the RF synthesisers are operated with maximum gain (i.e. ISET1/2 tied to RFV_{SS})
- The loop filter components should be optimised for each VCO

6.12 Digital System Clock Generators

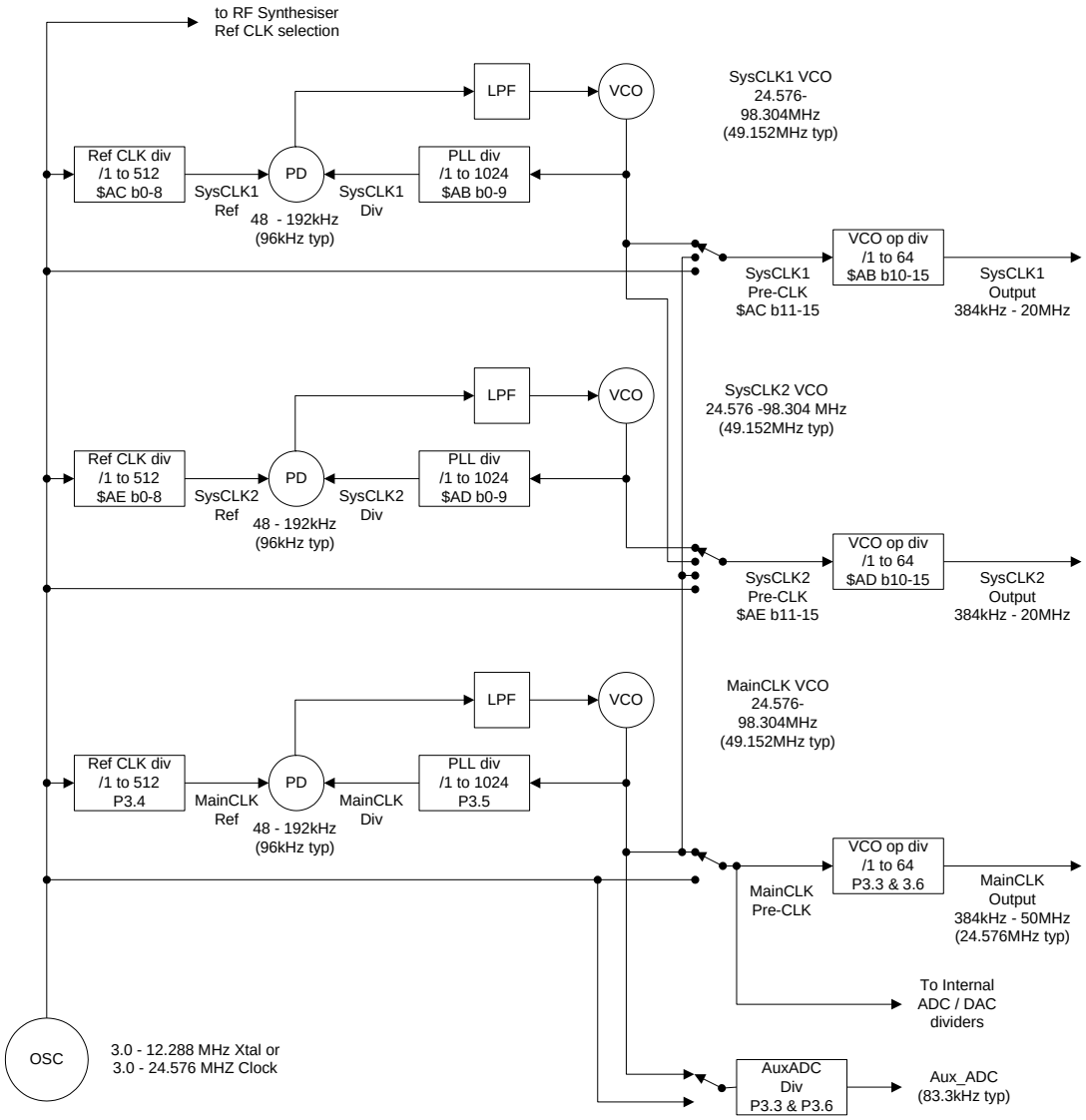


Figure 26 Digital Clock Generation Schemes

The CMX7131/CMX7141 includes a two-pin crystal oscillator circuit. This can either be configured as an oscillator, as shown in section 4.2, or the XTAL input can be driven by an externally generated clock. The crystal (Xtal) source frequency can go up to 12.288MHz (clock source frequency up to 24.576MHz), but a 19.2MHz oscillator is assumed by default for the functionality provided in the CMX7131/CMX7141.

6.12.1 Main Clock Operation

A digital PLL is used to create the Main Clock (nominally 24.576MHz in Tx, 49.152MHz in Rx) for the internal sections of the CMX7131/CMX7141. At the same time, other internal clocks are generated by division of either the XTAL Reference Clock or the Main Clock. These internal clocks are used for determining the sample rates and conversion times of A-to-D and D-to-A converters, running a General Purpose Timer and the signal processing block. In particular, it should be noted that in Idle mode the

setting of the GP Timer divider directly affects the C-BUS latency (with the default values this is nominally 250 µs).

The CMX7131/CMX7141 defaults to the settings appropriate for a 19.2MHz oscillator, however if other frequencies are to be used then the Program Block registers P3.2 to P3.6 will need to be programmed appropriately at power-on. This flexibility allows the device to re-use an external clock source, so reducing total cost and potential noise sources. A table of common values is provided in Table 11.

See:

- Program Block 3 – AuxDAC, RAMDAC and Clock Control

6.12.2 System Clock Operation

Two System Clock outputs, SYSCLK1 and SYSCLK2, are available to drive additional circuits, as required. These are digital phase locked loop (PLL) clocks that can be programmed via the System Clock registers with suitable values chosen by the user. The System Clock PLL Configure registers ($AB and $AD) control the values of the VCO Output divider and Main Divide registers, while the System Clock Ref. Configure registers ($AC and $AE) control the values of the Reference Divider and signal routing configurations. The PLLs are designed for a reference frequency of 96kHz. If not required, these clocks can be independently powersaved. The clock generation scheme is shown in the block diagram of Figure 26. Note that at power-on, these pins are disabled.

See:

- System CLK 1 and 2 PLL data - $AB, $AD write
- System CLK 1 and 2 REF - $AC and $AE write

6.13 Signal Level Optimisation

The internal signal processing of the CMX7131/CMX7141 will operate with wide dynamic range and low distortion only if the signal level at all stages in the signal processing chain is kept within the recommended limits. For a device working from a 3.3 V ±10% supply, the maximum signal level which can be accommodated without distortion is [(3.3 x 90%) - (2 x 0.3 V)] volts pk-pk = 838 mVrms, assuming a sine wave signal. This should not be exceeded at any stage.

6.13.1 Transmit Path Levels

For the maximum signal out of the MOD1 and MOD2 attenuators, the signal level at the output of the Modem block is set to be 0 dB, The Fine Output adjustment ($C3) has a maximum attenuation of 1.8 dB and no gain, whereas the Coarse Output adjustment ($B0) has a variable attenuation of up to 12.0 dB and no gain.

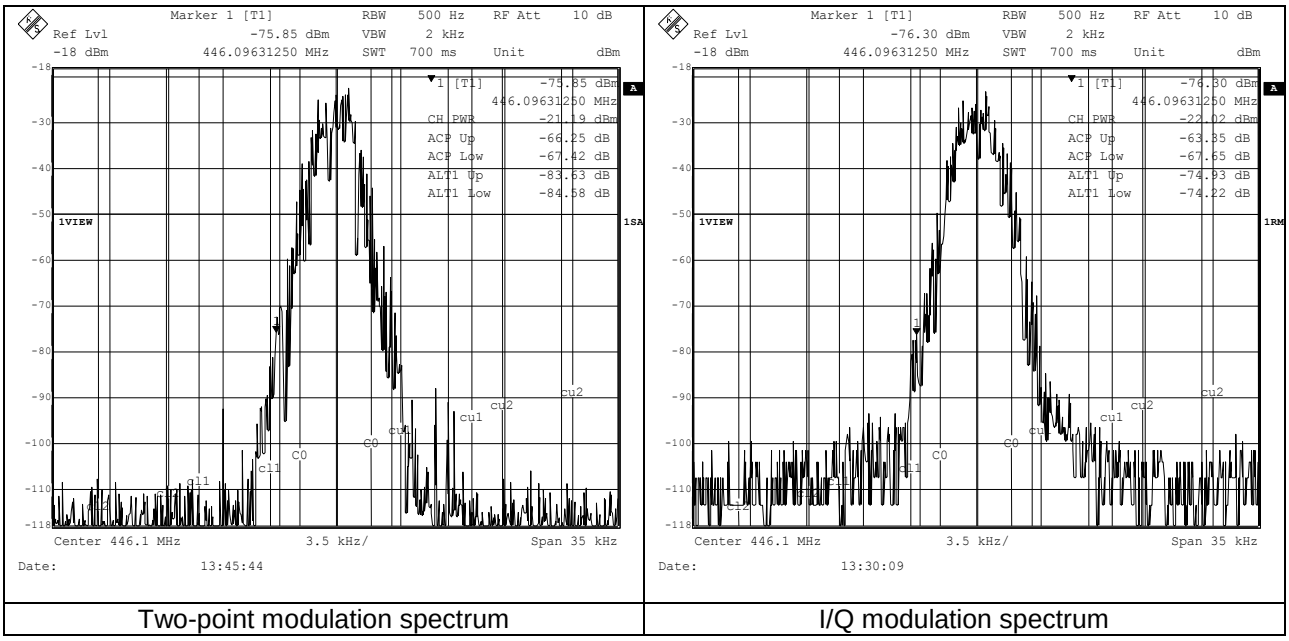
6.13.2 Receive Path Levels

The Coarse Input adjustment ($B1) has a variable gain of up to +22.4 dB and no attenuation. In LD mode, with the lowest gain setting (0 dB), the maximum allowable input signal level at the DISCFB pin would be 838 mVrms. This signal level is an absolute maximum, which should not be exceeded.

In I/Q mode CMX7131/CMX7141 automatically manages the gain control settings to optimise signal levels.

6.14 Tx Spectrum Plots

The following figure shows the Tx spectrum when using a suitable signal generator as measured on a spectrum analyser using the CMX7131/CMX7141 internal PRBS generator. Note that the I/Q mode is sensitive to variations in dc offset in the modulation path and these must be minimised.



Two-point modulation spectrum	I/Q modulation spectrum

Figure 27 Tx Modulation Spectra – 4800 bps

6.15 C-BUS Register Summary

Table 18 C-BUS Registers

ADDR. (hex)		REGISTER	Word Size (bits)
$01	W	C-BUS RESET	0
$A7	W	AuxADC Configuration	16
$A8	W	AuxDAC Data and Control	16
$A9	R	AuxADC1 Data and Threshold Status/Checksum 2 hi	16
$AA	R	AuxADC2 Data and Threshold Status/Checksum 2 lo	16
$AB	W	SYSCLK 1 PLL Data	16
$AC	W	SYSCLK 1 Ref	16
$AD	W	SYSCLK 2 PLL Data	16
$AE	W	SYSCLK 2 Ref	16
$AF		*reserved*	
$B0	W	Analogue Output Gain	16
$B1	W	Input Gain and Signal Routing	16
$B2	W	RF Synthesiser Data (CMX7131 only)	16
$B3	W	RF Synthesiser Control (CMX7131 only)	16
$B4	R	RF Synthesiser Status (CMX7131 only)	8
$B5	W	TxData 0	16
$B6	W	TxData 1	16
$B7	W	TxData 2	16
$B8	R	RxData 0/Checksum 1 hi	16
$B9	R	RxData 1/Checksum 1 lo	16
$BA	R	RxData 2	16
$BB	R	RxData 3	16
$BC		*reserved*	
$BD		*reserved*	
$BE		*reserved*	
$BF		*reserved*	
$C0	W	Power Down Control	16
$C1	W	Modem Control	16
$C2	W	TxAuxData Write	16
$C3	W	Analogue Gain	16
$C4		*reserved*	
$C5	R	Rx Data 4	16
$C6	R	IRQ Status	16
$C7	W	Modem Configuration	16
$C8	W	Programming Register	16
$C9	R	Modem Status	16
$CA	W	Tx Data 3	16
$CB	W	Tx Data 4	16
$CC	R	RxAuxData Read	16
$CD	W	Aux Config	16
$CE	W	Interrupt Mask	16
$CF		*reserved*	

All other C-BUS addresses (including those not listed above) are either reserved for future use or allocated for production testing and must not be accessed in normal operation.

7 Performance Specification

7.1 Electrical Performance

7.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Unit
Supply: DV_{DD} - DV_{SS}	–0.3	4.5	V
AV_{DD} - AV_{SS}	–0.3	4.5	V
RFV_{DD} - RFV_{SS} (CMX7131 only)	–0.3	4.5	V
CPV_{DD}- RFV_{SS} (CMX7131 only)	–0.3	4.5	V
Voltage on any pin to DV_{SS}	–0.3	DV_{DD} + 0.3	V
Voltage on any pin to AV_{SS}	–0.3	AV_{DD} + 0.3	V
Current into or out of any power supply pin (excluding VBIAS) (i.e. VDEC, AVDD, AVSS, DVDD, DVSS, CPVDD, RFVDD or RFVSS	–30	+30	mA
Current into or out of any other pin	–20	+20	mA
Voltage differential between power supplies:			
DV_{DD} and AV_{DD} or CPV_{DD}	0	0.3	V
AV_{DD} and CPV_{DD} (CMX7131 only)	0	0.3	V
DV_{SS} and AV_{SS} or RFV_{SS} (CMX7131)	0	50	mV
AV_{SS} and RFV_{SS} (CMX7131 only)	0	50	mV

L4 Package (48-pin LQFP)	**Min.**	**Max.**	**Unit**
Total Allowable Power Dissipation at T_{AMB} = 25°C	–	1600	mW
... Derating	–	16	mW/°C
Storage Temperature	–55	+125	°C
Operating Temperature	–40	+85	°C

Q3 Package (48-pin VQFN)	**Min.**	**Max.**	**Unit**
Total Allowable Power Dissipation at T_{AMB} = 25°C	–	1750	mW
... Derating	–	17.5	mW/°C
Storage Temperature	–55	+125	°C
Operating Temperature	–40	+85	°C

L9 Package (64-pin LQFP)	**Min.**	**Max.**	**Unit**
Total Allowable Power Dissipation at T_{AMB} = 25°C	–	1690	mW
... Derating	–	16.9	mW/°C
Storage Temperature	–55	+125	°C
Operating Temperature	–40	+85	°C

Q1 Package (64-pin VQFN)	**Min.**	**Max.**	**Unit**
Total Allowable Power Dissipation at T_{AMB} = 25°C	–	3500	mW
... Derating	–	35	mW/°C
Storage Temperature	–55	+125	°C
Operating Temperature	–40	+85	°C

7.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Unit
Supply Voltage:				
$DV_{DD} – DV_{SS}$		3.0	3.6	V
$AV_{DD} – AV_{SS}$		3.0	3.6	V
$CPV_{DD} – RFV_{SS}$ (CMX7131 only)		3.0	3.6	V
$RFV_{DD} – DV_{SS}$ (CMX7131 only)	3	2.25	2.75	V
$V_{DEC} – DV_{SS}$	2	2.25	2.75	V
Operating Temperature		–40	+85	°C
XTAL/CLK Frequency (using a Xtal)	1	3.0	12.288	MHz
XTAL/CLK Frequency (using an external clock)	1	3.0	24.576	MHz

Notes: 1 Nominal XTAL/CLK frequency is 19.2MHz.
2 The V_{DEC} supply is automatically derived from DV_{DD} by the on-chip voltage regulator.
3 The RFV_{DD} supply can be supplied from the V_{DEC} supply, if preferred.

7.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

External components as recommended in Figure 2.
Maximum load on digital outputs = 30 pF.
Xtal/Clock Oscillator Frequency = 19.2MHz ±0.01% (100ppm); T_{AMB} = –40°C to +85°C.
AV_{DD} = DV_{DD} = CPV_{DD} (CMX7131) = 3.0 V to 3.6 V; RFV_{DD} (CMX7131) = 2.25V to 2.75V
V_{DEC} = 2.5 V
Reference Signal Level = 308 mVrms at 1kHz with AV_{DD} = 3.3 V.
Signal levels track with supply voltage, so scale accordingly.
Signal-to-Noise Ratio (SNR) in bit rate bandwidth.
Input Stage Gain = 0 dB. Output Stage Attenuation = 0 dB.

Current consumption figures quoted in this section apply to the device when loaded with 7131/7141 FI-3.x only. The use of other Function Images™, can modify the current consumption of the device.

DC Parameters	Notes	Min.	Typ.	Max.	Unit
Supply Current	21				
All Powersaved					
DI_{DD}		–	8	100	µA
AI_{DD}		–	4	20	µA
Idle Mode	22				
DI_{DD}		–	1.4	–	mA
AI_{DD}	23	–	1.6	–	mA
Rx Mode	22				
DI_{DD} (4800 bps – search for FS)		–	4.7	–	mA
DI_{DD} (4800 bps – FS found)		–	2.8	–	mA
AI_{DD}		–	1.6	–	mA
Tx Mode	22				
DI_{DD} (4800 bps – 2-point)		–	4.3	–	mA
DI_{DD} (4800 bps – I/Q)		–	5.4	–	mA
AI_{DD} (AV_{DD} = 3.3 V)		–	1.5	–	mA
Additional Current for ach Auxiliary System Clock (output running at 4MHz)					
DI_{DD} (DV_{DD} = 3.3 V, V_{DEC} = 2.5 V)		–	250	–	µA
Additional Current for Each Auxiliary ADC					
DI_{DD} (DV_{DD} = 3.3 V, V_{DEC} = 2.5 V)		–	50	–	µA
Additional Current for Each Auxiliary DAC					
AI_{DD} (AV_{DD} = 3.3 V)		–	200	–	µA
Additional Current for Each RF Synthesiser	24				
CPI_{DD} + RFI_{DD} (CPV_{DD} = 3.3V, RFV_{DD} = 2.5V)		–	2.5	4.5	mA

Notes:

21 T_{AMB} =25°C. Not including any current drawn from the device pins by external circuitry.

22 System clocks, auxiliary circuits disabled, but all other digital circuits (including the Main Clock PLL) enabled.

23 May be further reduced by power-saving unused sections

24 When using the external components shown in Figure 24 and when supplying the current for RFV_{DD} from the regulated 2.5V digital (V_{DEC}) supply. The latter is derived from DV_{DD} by an on-chip voltage regulator.

DC Parameters (continued)	Notes	Min.	Typ.	Max.	Unit
XTAL/CLK	25				
Input Logic '1'		70%	–	–	DV_{DD}
Input Logic '0'		–	–	30%	DV_{DD}
Input Current (Vin = DV_{DD})		–	–	40	µA
Input Current (Vin = DV_{SS})		–40	–	–	µA
C-BUS Interface and Logic Inputs					
Input Logic '1'		70%	–	–	DV_{DD}
Input Logic '0'		–	–	30%	DV_{DD}
Input Leakage Current (Logic '1' or '0')		–1.0	–	1.0	µA
Input Capacitance		–	–	7.5	pF
C-BUS Interface and Logic Outputs					
Output Logic '1' (I_{OH} = 2mA)		90%	–	–	DV_{DD}
Output Logic '0' (I_{OL} = -5mA)		–	–	10%	DV_{DD}
"Off" State Leakage Current		–	–	10	µA
IRQN (Vout = DV_{DD})		–1.0	–	+1.0	µA
REPLY_DATA (output HiZ)		–1.0	–	+1.0	µA
V_{BIAS}	26				
Output Voltage Offset wrt $AV_{DD}/2$ (I_{OL} < 1µA)		–	±2%	–	AV_{DD}
Output Impedance		–	22	–	kΩ

Notes: 25 Characteristics when driving the XTAL/CLK pin with an external clock source.

26 Applies when utilising V_{BIAS} to provide a reference voltage to other parts of the system. When using V_{BIAS} as a reference, V_{BIAS} must be buffered. V_{BIAS} must always be decoupled with a capacitor as shown in Figure 2.

AC Parameters		Notes	Min.	Typ.	Max.	Unit
XTAL/CLK Input						
'High' Pulse Width		31	15	–	–	ns
'Low' Pulse Width		31	15	–	–	ns
Input Impedance (at 6.144MHz)						
Powered-up	Resistance		–	150	–	kΩ
	Capacitance		–	20	–	pF
Powered-down	Resistance		–	300	–	kΩ
	Capacitance		–	20	–	pF
Xtal Start up (from powersave)			–	20	–	ms
SYSCLK1/2 Outputs						
XTAL/CLK Input to SysClk1/2 Timing:						
(in high to out high)		32	–	15	–	ns
(in low to out low)		32	–	15	–	ns
'High' pulse width		33	76	81.38	87	ns
'Low' pulse width		33	76	81.38	87	ns
V_{BIAS}						
Start Up Time (from powersave)			–	30	–	ms
Microphone, Alternative and Discriminator Inputs (MIC, ALT, DISC)						
Input Impedance		34	–	>10	–	MΩ
Maximum Input Level (pk-pk)		35	–	–	80%	AV_{DD}
Load Resistance (feedback pins)			80	–	–	kΩ
Amplifier Open Loop Voltage Gain (I/P = 1mVrms at 100 Hz)			–	80	–	dB
Unity Gain Bandwidth			–	1.0	–	MHz
Programmable Input Gain Stage		36				
Gain (at 0dB)		37	−0.5	0	+0.5	dB
Cumulative Gain Error (wrt attenuation at 0dB)		37	−1.0	0	+1.0	dB

Notes:

31 Timing for an external input to the XTAL/CLK pin.

32 XTAL/CLK input driven by an external source.

33 6.144MHz Xtal fitted and 6.144MHz output selected (scale for 19.2MHz).

34 With no external components connected, measured at dc.

35 Centered about $AV_{DD}/2$; after multiplying by the gain of input circuit (with external components connected).

36 Gain applied to signal at output of buffer amplifier: DISCFB, ALTFB or MICFB

37 Design value. Overall attenuation input to output has a tolerance of 0 dB ±1.0 dB

AC Parameters	Notes	Min.	Typ.	Max.	Unit
Modulator Outputs 1/2 and Audio Output (MOD1, MOD2, AUDIO)					
Power-up to Output Stable	41	–	50	100	µs
Modulator Attenuators					
Attenuation (at 0dB)	43	−1.0	0	+1.0	dB
Cumulative Attenuation Error (wrt attenuation at 0dB)		−0.6	0	+0.6	dB
Output Impedance Enabled	42	–	600	–	Ω
Output Impedance Disabled	42	–	500	–	kΩ
Output Current Range (AV_{DD} = 3.3 V)		–	–	±125	µA
Output Voltage Range	44	0.5	–	AV_{DD} –0.5	V
Load Resistance		20	–	–	kΩ
Audio Attenuator					
Attenuation (at 0dB)	43	−1.0	0	+1.0	dB
Cumulative Attenuation Error (wrt attenuation at 0dB)		−1.0	0	+1.0	dB
Output Impedance Enabled	42	–	600	–	Ω
Output Impedance Disabled	42	–	500	–	kΩ
Output Current Range (AV_{DD} = 3.3 V)		–	–	±125	µA
Output Voltage Range	44	0.5	–	AV_{DD} –0.5	V
Load Resistance		20	–	–	kΩ

Notes:

41 Power-up refers to issuing a C-BUS command to turn on an output. These limits apply only if V_{BIAS} is on and stable. At power supply switch-on, the default state is for all blocks, except the XTAL and C-BUS interface, to be in placed in Powersave mode.

42 Small signal impedance, at AV_{DD} = 3.3 V and T_{AMB} = 25°C.

43 With respect to the signal at the feedback pin of the selected input port.

44 Centered about AV_{DD} /2; with respect to the output driving a 20 kΩ load to AV_{DD}/2.

AC Parameters (cont.)	Notes	Min.	Typ.	Max.	Unit
Auxiliary Signal Inputs (Aux ADC 1 to 4)					
Source Output Impedance	51	–	–	24	kΩ
Auxiliary 10 Bit ADCs					
Resolution		–	10	–	Bits
Maximum Input Level (pk-pk)	54	–	–	80%	AV_{DD}
Conversion Time	52	–	250	–	µs
Input Impedance					
Resistance	57	–	>10	–	MΩ
Capacitance		–	5	–	pF
Zero Error	55	0	–	±10	mV
Integral Non-linearity		–	–	±3	LSBs
Differential Non-linearity	53	–	–	±1	LSBs
Auxiliary 10 Bit DACs					
Resolution		–	10	–	Bits
Maximum Output Level (pk-pk), no load	54	80%	–	–	AV_{DD}
Zero Error	56	0	–	±10	mV
Resistive Load		5	–	–	kΩ
Integral Non-linearity		–	–	±4	LSBs
Differential Non-linearity	53	–	–	±1	LSBs

Notes:

51 Denotes output impedance of the driver of the auxiliary input signal, to ensure <1 bit additional error under nominal conditions.

52 With an auxiliary clock frequency of 6.144MHz.

53 Guaranteed monotonic with no missing codes.

54 Centred about $AV_{DD}/2$.

55 Input offset from a nominal V_{BIAS} input, which produces a $0200 ADC output.

56 Output offset from a $0200 DAC input, measured with respect to a nominal V_{BIAS} output.

57 Measured at dc.

AC Parameters (cont.)	Notes	Min.	Typ.	Max.	Unit
RF Synthesisers – Phase Locked Loops					
Reference Clock Input					
Input Logic '1'	62	70%	–	–	RFV_{DD}
Input Logic '0'	62	–	–	30%	RFV_{DD}
Frequency	64, 66	5.0	19.2	40.0	MHz
Divide Ratios (R)	63	2	–	8191	
Each RF Synthesiser	69				
Comparison Frequency		–	–	500	kHz
Input Frequency Range	67	100	–	600	MHz
Input Level		−15	–	0	dBm
Input Slew Rate		14	–	–	V/µs
Divide Ratios (N)		1088	–	1048575	
1Hz Normalised Phase Noise Floor	68	–	−197	–	dBc/Hz
Charge Pump Current (high)	65	±1.88	±2.5	±3.3	mA
Charge Pump Current (low)	65	±470	±625	±820	µA
Charge Pump Current – voltage variation		–	10%	–	per V
Charge Pump Current – sink to source match		–	5%	–	of ISET

Notes:

62 Square wave input.

63 Separate dividers are provided for each PLL.

64 For optimum performance of the synthesiser subsystems, a common master clock should be used for the RF synthesisers and the baseband sections. Using unsynchronised clocks is likely to result in spurious products being generated in the synthesiser outputs and in some cases difficulty may be experienced in obtaining lock in the RF Synthesisers.

65 External ISET1/2 resistor (R31 in Figure 24) = 0Ω (Internal ISET resistor = 9k6Ω nominally).

66 Lower input frequencies may be used subject to division ratio requirements being maintained.

67 Operation outside these frequency limits is possible, but not guaranteed. At lower frequencies slew rate needs to be considered.

68 1Hz Normalised Phase Noise Floor (PN1Hz) can be used to calculate the phase noise within the PLL loop by:
Phase Noise (in-band) = $PN1Hz + 20\log_{10}(N) + 10\log_{10}(f_{comparison})$

69 It is recommended that RF Synthesiser 1 be used for the higher frequency use (e.g. RF 1st LO) and RF Synthesiser 2 be used for lower frequency use (e.g. IF LO).

7.1.4 Parametric Performance

For the following conditions unless otherwise specified:

External components as recommended in Figure 2.
Maximum load on digital outputs = 30 pF.
Oscillator Frequency = 19.2MHz ±0.01% (100ppm); T_{AMB} = –40°C to +85°C.
AV_{DD} = DV_{DD} = 3.0 V to 3.6 V.
Reference Signal Level = 308 mVrms at 1kHz with AV_{DD} = 3.3 V.
Signal levels track with supply voltage, so scale accordingly.
Signal-to-Noise Ratio (SNR) in Bit Rate Bandwidth.
Input Stage Gain = 0dB, Output Stage Attenuation = 0 dB.
All figures quoted in this section apply to the device when loaded with FI3.x only. The use of other Function Images™, can modify the parametric performance of the device.

AC Parameters (cont.)	Notes	Min.	Typ.	Max.	Unit
Modem Symbol Rate		2400	–	4800	sym s^{-1}
Modulation			4-FSK		
Filter (RC) Alpha		–	0.2	–	
Tx Output Level (MOD1, MOD2, 2-point)	70	–	2.88	–	Vpk-pk
Tx Output Level (MOD1, MOD2, I/Q)	70	–	2.20	–	Vpk-pk
Tx Adjacent Channel Power (MOD1, MOD2, prbs)	71, 73	-60	–	–	dB
Rx Sensitivity (BER 4800 sym s^{-1})	72	–	TBD	–	dBm
Rx Co-channel Rejection	71, 73	15	12	–	dB
Rx System Adjacent Channel Rejection (I/Q Mode)	74	–	63		dB
Rx Input Level		–	–	838	mVrms
Rx Input DC Offset		0.5	–	AV_{DD} - 0.5	V

Notes:

70	Transmitting continuous default preamble.
71	See section 6.14.
72	Measured at base-band – radio design will affect ultimate product performance.
73	For a 6.25kHz/4800 bps channel.
74	Combined performance of CMX7131/CMX7141 and CMX994 connected as shown in Figure 6 using EV9942 and PE0201; measurement method from EN 301 166.

7.2 C-BUS Timing

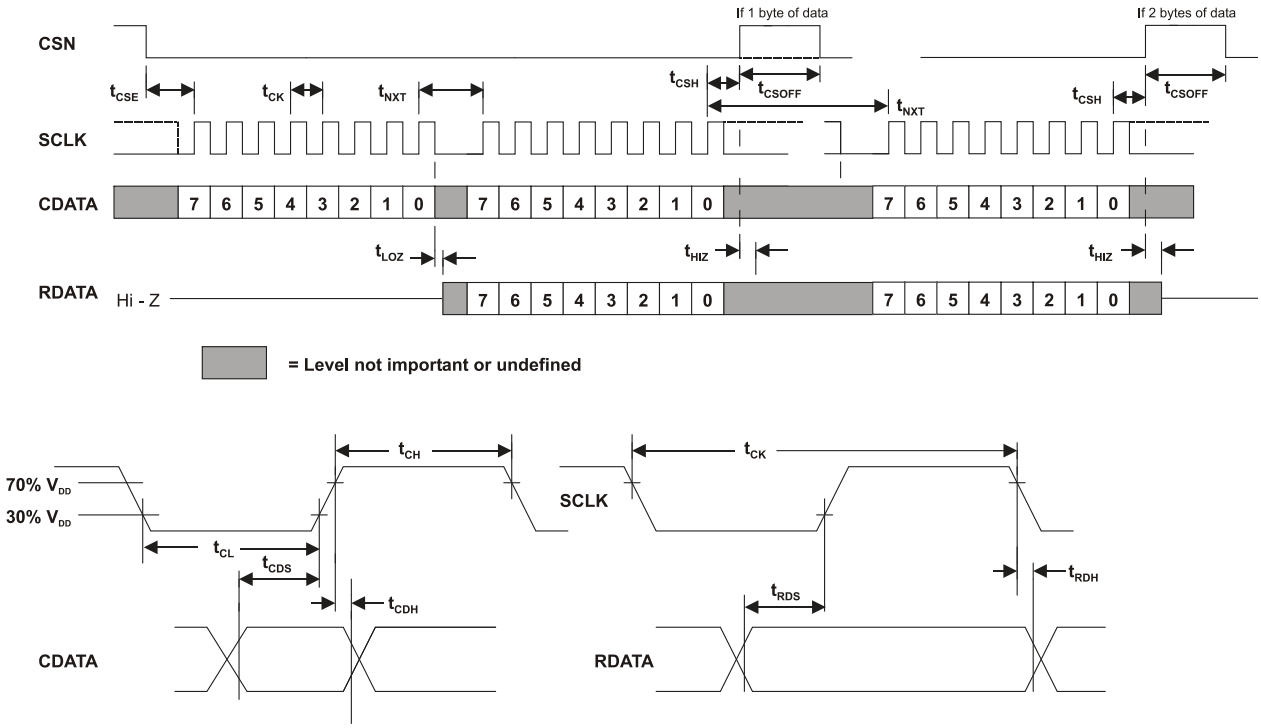


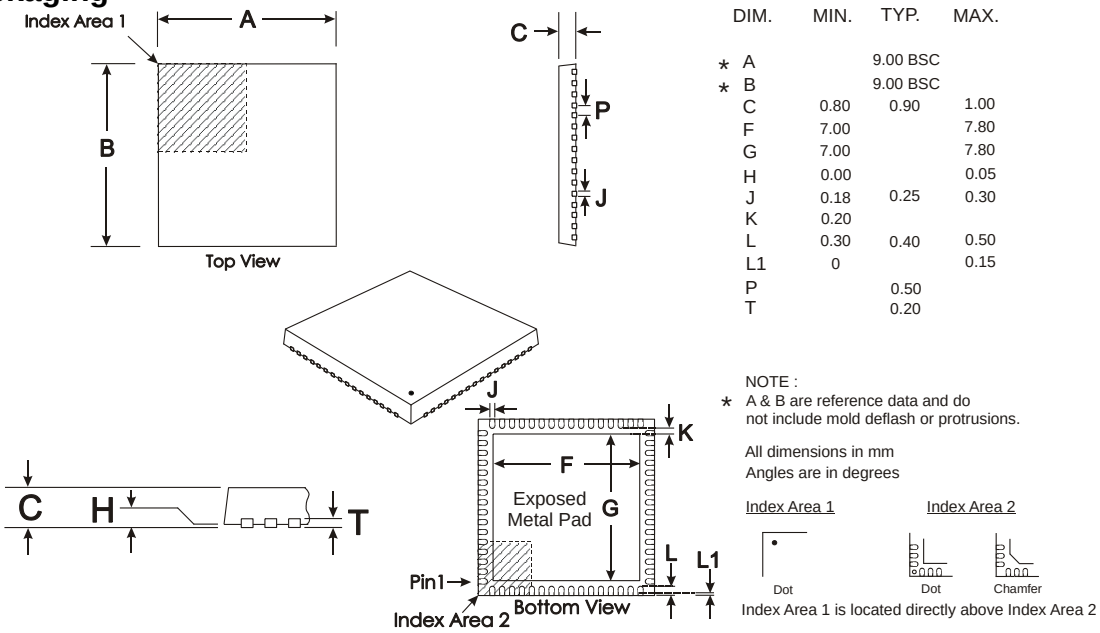
Figure 28 C-BUS Timing

C-BUS Timing		Notes	Min.	Typ.	Max.	Unit
t_{CSE}	CSN Enable to SCLK high time		100	–	–	ns
t_{CSH}	Last SCLK high to CSN high time		100	–	–	ns
t_{LOZ}	SCLK low to RDATA Output Enable Time		0.0	–	–	ns
t_{HIZ}	CSN high to RDATA high impedance		–	–	1.0	µs
t_{CSOFF}	CSN high time between transactions		1.0	–	–	µs
t_{NXT}	Inter-byte time		200	–	–	ns
t_{CK}	SCLK cycle time		200	–	–	ns
t_{CH}	SCLK high time		100	–	–	ns
t_{CL}	SCLK low time		100	–	–	ns
t_{CDS}	CDATA setup time		75	–	–	ns
t_{CDH}	CDATA hold time		25	–	–	ns
t_{RDS}	RDATA setup time		50	–	–	ns
t_{RDH}	RDATA hold time		0	–	–	ns

Notes:
1. Depending on the command, 1 or 2 bytes of CDATA are transmitted to the peripheral MSB (Bit 7) first, LSB (Bit 0) last. RDATA is read from the peripheral MSB (Bit 7) first, LSB (Bit 0) last.
2. Data is clocked into the peripheral on the rising SCLK edge.
3. Commands are acted upon at the end of each command (rising edge of CSN).
4. To allow for differing µC serial interface formats C-BUS compatible ICs are able to work with SCLK pulses starting and ending at either polarity.
5. Maximum 30pF load on IRQN pin and each C-BUS interface line.

These timings are for the latest version of C-BUS and allow faster transfers than the original C-BUS timing specification. The CMX7131/CMX7141 can be used in conjunction with devices that comply with the slower timings, subject to system throughput constraints.

7.3 Packaging



DIM.	MIN.	TYP.	MAX.
* A		9.00 BSC	
* B		9.00 BSC	
C	0.80	0.90	1.00
F	7.00		7.80
G	7.00		7.80
H	0.00		0.05
J	0.18	0.25	0.30
K	0.20		
L	0.30	0.40	0.50
L1	0		0.15
P		0.50	
T		0.20	

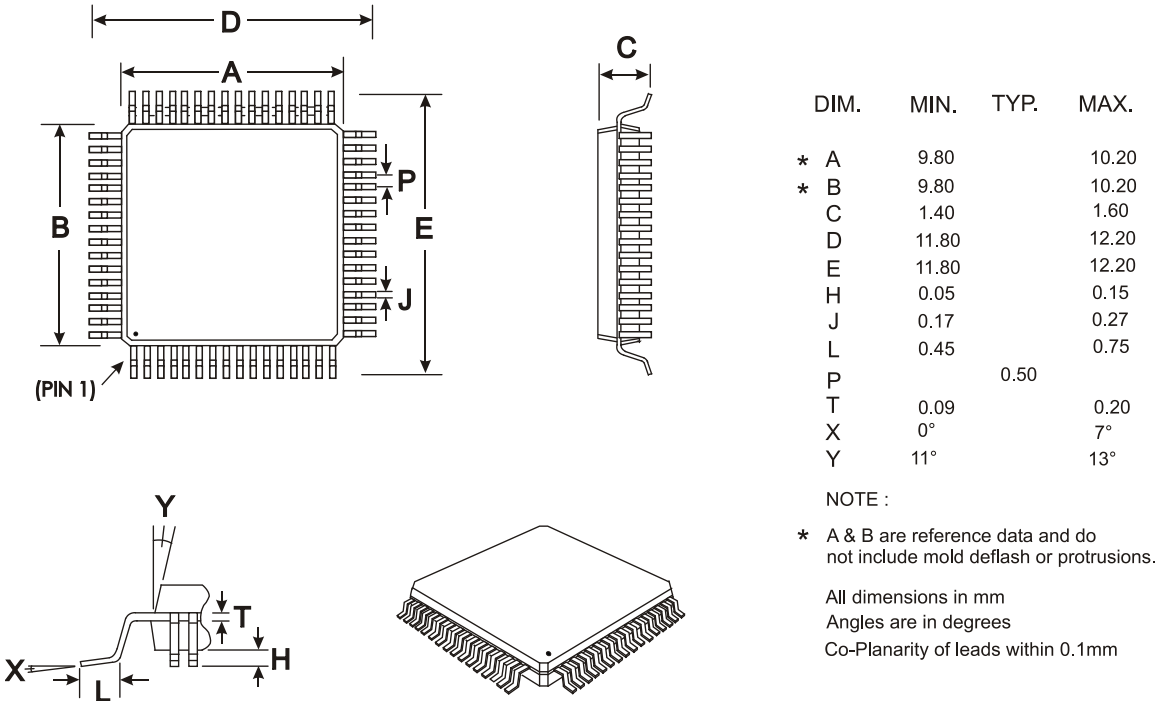
NOTE :
* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees

Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.
L minus L1 to be equal to, or greater than 0.3mm
The underside of the package has an exposed metal pad which should ideally be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

Figure 29 Mechanical Outline of 64-pin VQFN (Q1)

Order as part no. CMX7131Q1



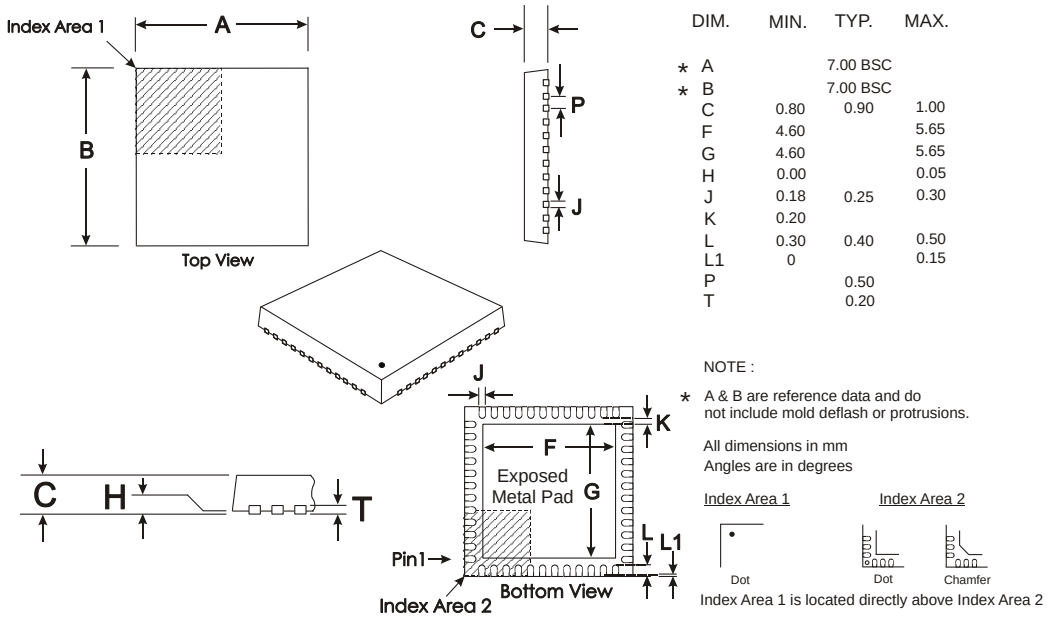
DIM.	MIN.	TYP.	MAX.
* A	9.80		10.20
* B	9.80		10.20
C	1.40		1.60
D	11.80		12.20
E	11.80		12.20
H	0.05		0.15
J	0.17		0.27
L	0.45		0.75
P		0.50	
T	0.09		0.20
X	0°		7°
Y	11°		13°

NOTE :
* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees
Co-Planarity of leads within 0.1mm

Figure 30 Mechanical Outline of 64-pin LQFP (L9)

Order as part no. CMX7131L9



DIM.	MIN.	TYP.	MAX.
* A		7.00 BSC	
* B		7.00 BSC	
C	0.80	0.90	1.00
F	4.60		5.65
G	4.60		5.65
H	0.00		0.05
J	0.18	0.25	0.30
K	0.20		
L	0.30	0.40	0.50
L1	0		0.15
P		0.50	
T		0.20	

NOTE :

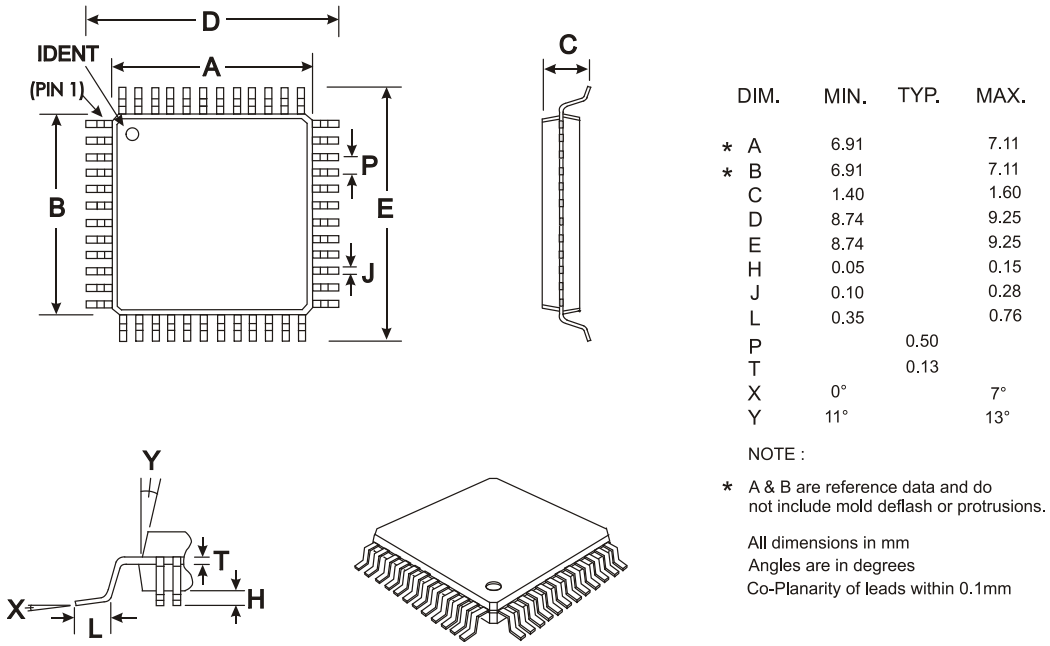
* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees

Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.
L minus L1 to be equal to, or greater than 0.3mm
The underside of the package has an exposed metal pad which should ideally be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

Figure 31 Mechanical Outline of 48-pin VQFN (Q3)

Order as part no. CMX7141Q3



DIM.	MIN.	TYP.	MAX.
* A	6.91		7.11
* B	6.91		7.11
C	1.40		1.60
D	8.74		9.25
E	8.74		9.25
H	0.05		0.15
J	0.10		0.28
L	0.35		0.76
P		0.50	
T		0.13	
X	0°		7°
Y	11°		13°

NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees
Co-Planarity of leads within 0.1mm

Figure 32 Mechanical Outline of 48-pin LQFP (L4)

Order as part no. CMX7141L4

As package dimensions may change after publication of this datasheet, it is recommended that you check for the latest packaging information from the CML website: [www.cmlmicro.com].

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